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COVER STORY

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Wind River

Cybersecurity: the challenge of protecting critical assets

This article is presented by Wind River

As more and more devices connect to the Internet, the risk of security threats increases exponentially. As a result, security is now a fundamental concern for embedded systems, and extensive media coverage of threats such as Stuxnet-like worms has only heightened the sense of urgency. To address this need, Wind River has developed the strategies and tools necessary to implement an effective approach to embedded security.

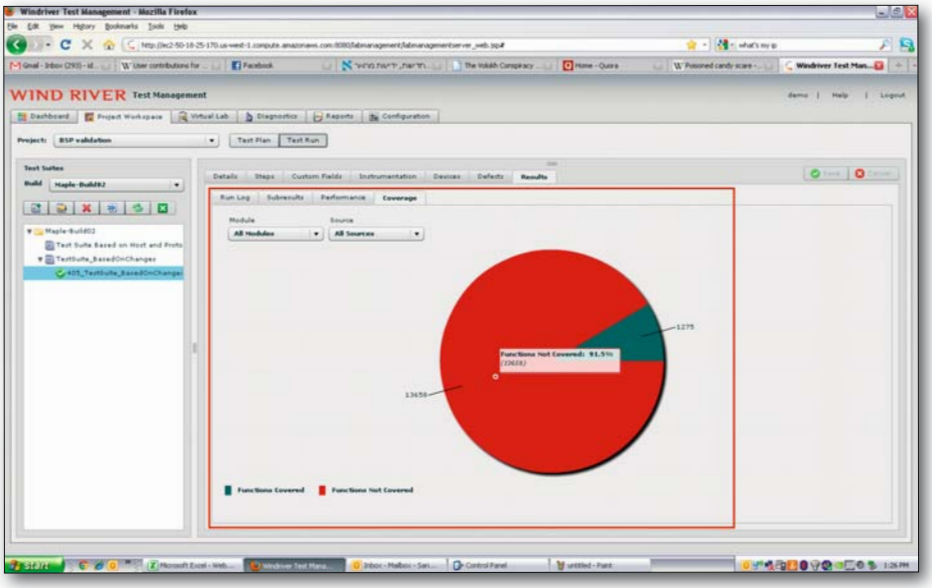
These threats have demonstrated the huge impact that can result for compromised systems. The consequences of similar attacks on critical infrastructure could be devastating - and in the case of safety-critical systems, life threatening. The reputation of an organization and brand can also suffer from a successful attack, as evidenced by recent cases in the media. When devices malfunction or sensitive information is stolen, the effect on the public trust is extremely damaging. Effective countermeasures must be implemented to prevent systems from being compromised and sensitive information from being stolen in a coordinated industrial espionage attack. To address this need, Wind River has developed the strategies and tools necessary to implement an effective approach to embedded security. With more than 30 years of experience in the development and certification of safe and secure solutions for critical infrastructure, our team understands the security challenges of embedded devices and has proven strategies to improve security in a broad range of deployment scenarios.

Today, there is a growing trend toward the adoption of internationally recognized security standards. Proven standards, such as the Common Criteria for the evaluation of systems, IEC 62351 for secure implementation of substation automation communication, and system robustness testing from Wurldtech Achilles certification, can be utilized to manage the risk. A broad range of tools and methodologies exists to support standards-based approaches to increasing the security of an embedded device. Alone, these technologies and processes can rarely provide adequate security for an embedded platform, but the creation of a layered security architecture comprised of these solutions can build a security strategy of significant depth to harden devices against security attacks.

Truly effective security must be designed into a device as a core requirement. Just as quality cannot be tested into a device, security requirements must be included as part of the device development process before it is released - but this is not always possible for devices in an existing infrastructure. Some security-hardening techniques address the retrofit use case that is applied to a device that has been deployed. This is suboptimal but may be adequate in controlled environments.

Designing in security is more likely to be successful and less expensive in both the short and long term. For example, installing an antivirus tool in a running device can be effective only if regular updates and system scans are planned along with the installation. Conscientiously analyzing the security threat landscape at the beginning of the project is always more efficient than trying to recover from damage that has already occurred. But choosing the appropriate combination of tools and the correct methodology can become extremely complex without a structured approach. A step-by-step process is most likely to lead to a successful layered security protection scheme in the product, and Wind River has the tools to help at every step.

The challenges in creating a secure embedded platform are different from enterprise security. An embedded device does not have the inherent protection of layered systems, such as dedicated firewalls and security devices, that are prevalent in traditional IT enterprise systems. Embedded devices are often deployed in remote and inaccessible areas, such as power control stations, oil pipelines, or hostile environments. Therefore, it is necessary to implement greater device intelligence to be able to react against external threats in an appropriate manner. An embedded device may have fewer resources available than a traditional IT enterprise system, making it difficult or even impossible to use traditional protection solutions such as antivirus protection. The desired level of protection must be balanced against what is attainable within the constraints of the device to achieve an appropriate degree of security as well as device performance. An embedded device in critical infrastructure has very clear uptime requirements. Bringing it down can cause protective functions to fail or critical processes to run into a dan-



Run-time test coverage reduces the risk of untested changes slipping through

gerous state. An IT system with an antivirus or white-listing function may prevent leaking data, but this method may turn out to be lethal on a critical device. Security is a dynamic process. Every day hundreds of new threats are discovered, so it is crucial to have a security architecture that can respond to new threats with agility. The security design process can be outlined in five key steps.

1. Threat Assessment: Security, as with safety, depends on following a disciplined process throughout the development life cycle. At the beginning of the project, it is important to understand the fundamental risk management issues such as the purpose of the device or asset, the value of the asset, its deployment environment, and the likely attack vectors to which it will be exposed. A good threat assessment will provide answers to the following questions: What are my security requirements and goals? What am I trying to protect - device functionalities (uptime, quality of service) or information (data in motion, data at rest)? Am I concerned about intellectual property protection (tampering)? What impact would the identified security threats have? What possible flaws are already present in the product's design? Are there mitigations that could already be applied, depending on the device use case? Are there secure coding standards available that help to reduce the introduction of vulnerabilities during implementation? Does the device need to comply with security certification standards such as Common Criteria and IEC 62351 or undergo Wurldtech Achilles certification?

2. Software Architecture and Design: Once the threat assessment has taken place and the requirements have been gathered, the system must be designed using an appropriate architecture sufficiently robust to counter all of the identified threats. A good design will ensure that the following key objectives are achieved: Identify known and consolidated software techniques to mitigate the threats identified in the assessment step. Avoid all the common programming mistakes that can introduce vulnerabilities and provide a hook for attackers. A trivial but dangerous example is copying data from one place to another without ensuring there is enough space in memory. A list of programming guidelines should be produced for developers to follow. These guidelines can also build a base for application testing. Depending on the threat environment, determine whether a secure boot scheme is required, as well as a secure management framework to enable secure updates to the system. Identify subsystems of the software architecture that differ in criticality based on their confidentiality, robustness, and life cycle requirements. Separation of these different levels of criticality can be required without adding to the hardware costs.

3. Run-Time Selection: Once the software architecture is defined, the next step is to select the appropriate runtime system. In addition to security requirements, there may be performance and safety certification requirements that will be determining factors in the selection. If a commercial off-the-shelf (COTS) product is selected, the vendor can usually offer assistance and support in responding to newly identified threats, reducing the burden on the device manufacturer. In addition, partitioning can increase security by isolating applications and offering multi-OS capabilities.

The run-time system should also provide a robust middleware foundation that allows trusted connectivity. This foundation can include func-

tions for authorization, authentication, and auditing. Depending on potential compliance requirements, Secure Socket Layer (SSL), firewalls, and cryptographic libraries may be needed to secure the communication. If the vendor has successfully undertaken security certifications of internationally recognized standards, it can gain more confidence in its secure design life cycle processes. Finally, a long-term support plan for the run-time, including security maintenance, is a simple way for a COTS vendor to plan the device life and ensure it will not be left without protection once deployed.

4. Application Protection: The core of an embedded system is the differentiating application. Since the application is on the front line, it must implement protection - running an insecure application on a secure system does not make any sense. Legacy designs should be reviewed and modified where necessary to take full advantage of the protection scheme. Extensive testing should be performed at both the unit and integration levels to provide assurance that the device can be deployed with no known vulnerabilities left open.

Testing the application against the most common threats ensures that nothing has been left behind, and a good testing scheme will also check against all the common programming errors that can leave the door open to malicious attacks: "Fuzz testing" uses out-of-spec parameters such as huge data flows to test against denial of service (DOS) attacks, malformed Internet addresses, and out-of-boundary data to prevent malicious code injection, and so on. It is extremely important to ensure that the software will handle these anomalous conditions without causing degradation in device performance.

5. Future Security Management: The system must be designed to be able to deal with not only current known threats but also future ones. From a practical standpoint, this means designing a system with a secure management framework so that updates to the device software can be deployed using a secure delivery process in a timely manner. This device management framework should also prevent any possibility of malicious software being deployed to the device. Consolidated techniques such as digital signatures can be used to verify that a payload update is genuine. The framework should also be capable of reporting alerts whenever a suspicious action is attempted or performed on the device.

Wind River offers a complete end-to-end framework to protect embedded devices against malicious intents; we also work with our customers to address their requirements for asset protection, confidentiality, and continuous risk mitigation for development and deployment scenarios. At every step in the security planning process, Wind River has the tools and solutions to help. In the threat assessment phase, we provide dedicated training, security architecture studies, and consultancy for specific security regulations on existing projects or on new designs. Wind River also offers a range of run-time solutions to address the requirements of different vertical markets, including certification to internationally recognized safety and security standards. The run-time offerings include VxWorks-based solutions for various markets and requirements, as well as security enhanced run-time systems based on open source technology, such as SE Linux and SE Android. These capabilities are complemented by a safe and secure partitioning platform that helps to mix and manage different levels of criticality and operating environments without additional hardware cost. In addition, we provide dedicated guides that enable customers to configure our operating systems and the associated middleware to minimize the risk of exposing the system to threats.

All customers benefit from our Security Vulnerability Response Policy, which defines the internal process used by our dedicated security team for proactively monitoring security threats that may affect our products. Threats are continually assessed to determine if they impact our products; if they are found to do so, a patch is published and posted on the support website. During the development phase, we offer a number of tools that are able to detect vulnerabilities, including Wind River Test Management. Test Management identifies non-executed or non-tested code, exposing potentially insecure parts of the application, and can be extended to perform white-hat attacks and fuzz testing using proven technology. Finally, Wind River Professional Services can assist with the implementation or integration of a secure system management framework to allow trusted delivery of updated firmware and application code as well as the integration of third-party products, such as intrusion detection systems or white-listing frameworks, to increase the robustness of the deployed device. ■

Product News

■ SEGGER: free SWO monitor for J-Link

SEGGER introduces SWOViewer – a new, free-of charge utility for debug emulator J-Link. This utility displays the terminal output of the target using the SWO pin. SWOViewer can be used without a debugger to capture terminal output independently from the debugger. Additionally, it can be run side by side with a debugger which does not support terminal output via SWO, such as GDB or GDB/Eclipse.

News ID 16247

■ Wind River introduces software platform for 'Internet of Things'

Wind River introduces Wind River Intelligent Device Platform, a complete software development environment built exclusively for M2M applications. The platform addresses the security, connectivity, and manageability required for M2M device development. It provides pre-integrated off-the-shelf components that can significantly reduce a manufacturer's development time.

News ID 16141

■ MathWorks updates Stateflow to simplify control logic design in Simulink

MathWorks announces a new version of Stateflow in R2012b that simplifies control logic design. A new Stateflow Editor, state transition tables, and MATLAB as an action language, help engineers build applications like supervisory control, task scheduling, and fault management more efficiently.

News ID 16332

■ Green Hills adds AUTOSAR support to INTEGRITY RTOS

Green Hills Software announces the availability of an AUTOSAR compatible API for its INTEGRITY real-time operating system. The availability of the new AUTOSAR API combined with the existing rich set of standard APIs for OSEK and POSIX – provides automobile manufacturers a clear path to address the growing dilemma of ECU complexity facing vehicles today.

News ID 16331

■ Express Logic: ThreadX RTOS supports Critical Link's MityDSP-L138F board

Express Logic's ThreadX RTOS now supports Critical Link's MityDSP-L138 board. Critical Link's MityDSP-L138F system-on-module combines a TI C674x floating point DSP, an ARM9 processor, and an optional FPGA. ThreadX is the first and only RTOS that runs on both the MityDSP's ARM9 and the TI C674x. This gives developers the unique opportunity to migrate applications from one processor to the other as needed without changing application code.

News ID 16262

Embedded system access – changing the paradigm of electrical test

By Thomas Wenzel and Heiko Ehrenberg, Göpel electronic

This article shows how the trend of employing non-invasive test access strategies, initiated in 1990 with the ratification of IEEE Standard 1149.1, has spawned a number of new test technologies and methodologies, which have combined to give birth to the category of embedded system access techniques.

Figure 1. Control of ESA applications through external hardware and software

The test of electronic circuits has been a key topic in the industry since the first transistor was developed, and today it is as relevant as ever. Test strategies are graded by how close they come to the ideal test solution which doesn't add any cost to the product under test, neither during the design nor during production. Most of us agree that product testing is absolutely necessary, as part of design validation, as a quality indicator for manufacturing process control, or for the detection of defective products prior to shipping to a customer. However, we do have certain requirements that should be met by our test solutions: test development and execution should be fully automated and should be done in essentially no time, we want the test equipment to be very inexpensive, and we want fault coverage of 100%.

Industry trends give cause for concern, though, considering that the cost of test today can be a significant part of the overall development and manufacturing cost. Responsible for this development are primarily the complexity, high-speed designs, and the lack of available test access in many printed circuit board assemblies (PCBAs), or boards for short. The combined forces of these characteristics result in systematic changes in the balance of product design and product test. We start to see a correlation between problems seen in chip test and those seen in board test.

While boards look more like integrated circuits (IC) due to the loss of access to internal circuit nodes, the rapid development of three-dimensional (3D) ICs with multi-die integration results in structures that are similar to boards and systems. The 3D board with very little physical access seems to be looming on the horizon. At the same time, the combination of new packaging and integration technologies results in hitherto unaccustomed complexity. While several years ago multiple boards were necessary to create complete system designs, today some such systems can be realized in integrated circuits as System-on-Chip (SoC) or System-In-Package (SIP) designs. As a result, board size can be minimized and new possibilities are available to create super-complex systems. No matter how a design is arranged, however, from the perspective of test engineering the fundamental question is how such highly complex systems can be tested appropriately and efficiently and how one can take advantage of synergies between chip test and board test approaches.

Divide and conquer is a wise strategy that is also well suited for the test arena. Partitioning circuit structures into testable elements is a prerequisite for a successful test strategy. This is one of the reasons why in-circuit test (ICT) became so successful for board level tests. ICT approached circuit test structurally and tests components individually, however, the required bed-of-nail based invasive test access is becoming a big dilemma with modern boards. Test access problems were predictable, which resulted in the creation of IEEE Standard 1149.1 in 1990. Developed by the Joint Test Action Group (JTAG), this standard moves the so-called pin-electronics of a tester into the unit under test (UUT) in order to enable non-invasive test access without bed-of-nail adapters. This design-integrated pin-electronics is controlled through the JTAG test bus. This test bus needs to be incorporated into the unit under test by the board designer, providing test access available implicitly rather than being an afterthought.

The brilliance of IEEE Standard 1149.1 is the open expandability of its register architecture combined with the universal test bus interface (test access port, TAP) and its protocol definition. These properties allowed IEEE Standard 1149.1 to become the base technology for new non-intrusive methodologies and standards for testing, debugging, programming, and emulation. As a result, the portfolio of test access strategies at the board level has definitively changed. Today we can differentiate three principal classes of access strategies: native connector access (access through design-integrated I/O interfaces), intrusive board access (access through physical test nails and probes), and

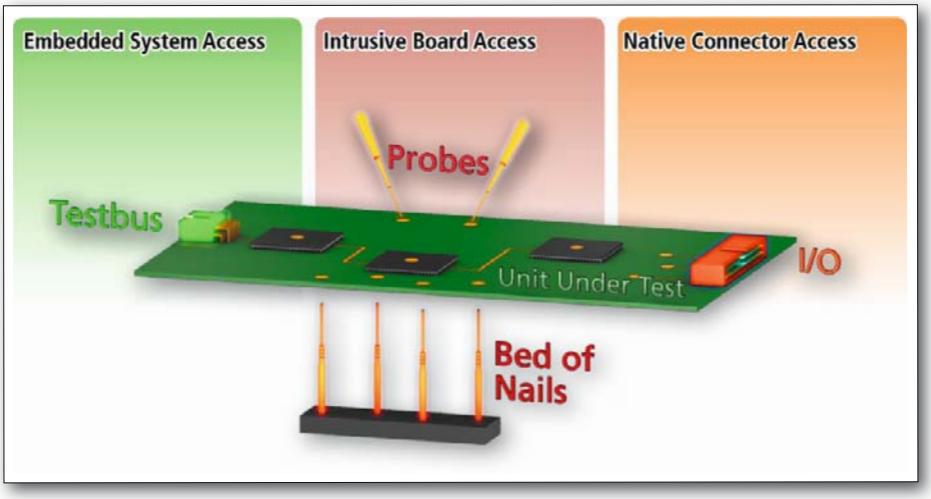


Figure 2. Classification of electrical test access strategies at board level

embedded system access (access through design-integrated test bus). While these classes are not mutually exclusive in their practical utilization, the applicability of an actual combination of these access strategies depends on the individual capabilities of the chosen automated test equipment (ATE) platform. So, how do these access strategies relate to each other and what does embedded system access (ESA) mean practically?

A look at the qualitative development of trends for the various access strategies reveals interesting facts, including the long adoption period of IEEE Standard 1149.1 as the first representative for embedded system access. Only recently, in 2008, has the boundary-scan industry reached annual sales of around 29 million US dollars, while sales of intrusive ATE were in the range of 500 million US dollars. On the other hand, we now see the manifestation of a rapid transition from intrusive access strategies to embedded system access. The accelerated adoption of embedded system access in the market is primarily owed to the fact that it is now a class by itself comprising a variety of non-invasive access technologies, including: boundary-scan test (IEEE Std 1149.1/.4/.6/.7), processor-emulation test (PET), chip-embedded instrumentation (IJTAG, IEEE P1687), in-system programming (ISP), core-assisted programming (CAP), FPGA-assisted Test (FAT), FPGA-assisted programming (FAP), and system JTAG (SJTAG) just to name a few. In addition, there are a number of other technologies and standards, such as the so-named on-chip emulation (OCE) for software validation.

The electrical access embedded in the target system allows embedded system access to work without invasive test nails and probes. In principle, every ESA technology utilizes a task-specific pin-electronic which is controlled by the test bus and, as a result, can directly execute test functions and programming routines in the target system. This target system can be an individual chip, a board, or a complete system assembly; embedded system access can be utilized throughout the entire product life cycle. A detailed analysis of key ESA technologies at the board level reveals considerable differences in operation and goals. Table 1 reflects the complementary character of the various technologies and, as the following discussion will further explain, it becomes clear how important it is for ATE platforms to support all these ESA technologies alike.

Property	Boundary Scan Test	Processor Emulation Test	Chip embedded Instruments	FPGA Assisted Test
Test type	structural	functional	open*	open*
Test speed	static	dynamic	open*	open*
Access through	Boundary-Scan IC	Processor	IJTAG-IC	FPGA
Pin-electronics	Boundary-Scan-Register	System bus	IP-Interface	IP-Interface
Configurable IP**	no	no	open*	yes
Fault coverage	static	dynamic	open*	open*
Level of diagnostics	Pin	Net/Pin	open*	open*
Related IEEE standard	IEEE Std 1149.x	IEEE Std 1149.7 / ISTO 5001	IEEE Std 1149.1, IEEE Std 1149.7, IEEE P1687	IEEE Std 1149.1, IEEE Std 1149.7, IEEE P1687

* depending on the implementation ** Intellectual Property

Table 1. Comparing ESA technologies relevant to board level test

Boundary-scan utilizes so-named boundary-scan cells, combined into a boundary-scan register, as primary access points for a target system circuit nodes. The boundary-scan register is accessed and controlled through the test access port (TAP). All vectors are scanned serially. The test bus is comprised of four mandatory signals and a fifth optional reset signal. Boundary-scan is a structural methodology and provides excellent fault diagnostics, especially for connectivity tests on BGA devices, for example. However, since boundary-scan tests are static in nature, dynamic defects usually cannot be detected, let alone be diagnosed. In addition to IEEE Standard 1149.1, various related standards have been created or are in development.

Processor emulation test (PET) utilizes the debug interface (implemented in many microprocessors for software validation) to transform the processor core temporarily into a native test controller. The processor and its system bus interface become the pin-electronics used as access points for the connected circuitry in the target systems. Remote-controlled through the JTAG interface or some other debug interface, the processor core utilizes write and read access to the system bus with respective test vectors in order to manipulate and test the connected internal and external resources and components. No operating system or flash firmware is necessary to accomplish this. PET can detect both static and dynamic defects, however diagnostics are limited due to the functional test approach. PET complements boundary scan very well and enables or improves especially the test of dynamic components such as DDR-SDRAM, Gigabit interfaces, and other non-scannable components at chip, board, and system level. One of the various solutions available for processor emulation test is the VarioTAP technology.

Chip-embedded Instruments are test and measurement intellectual property (IP) blocks integrated into ICs, often accessible through the JTAG port. The functionality of chip-embedded instruments is completely open and ranges from simple sensors, over complex signal processing and data collection, and all the way to complete analysis instruments and programming engines. The IP is either integrated permanently in the chip (hard macro), or it can be temporarily instantiated and configured (soft macro) in field-programmable gate arrays (FPGA). As a result, the pin-electronics are unrestricted in principle and can provide a

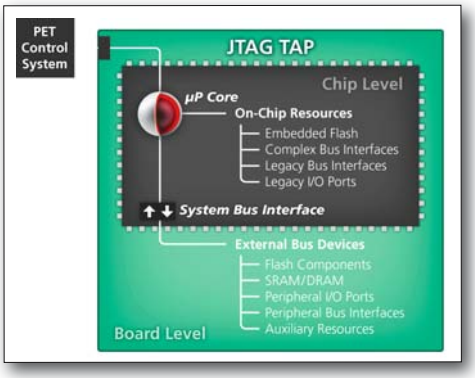


Figure 3. Principle of processor emulation test (PET)

wide variety of functionality, within the frame and scope of the respective technology of the host device, of course. Also noteworthy is the fact that such chip-embedded instruments can in principle be active during normal system operation, which enables interesting test and debug applications. FPGA-embedded instruments in particular have enjoyed strong interest recently. By enabling strategies such as FPGA-assisted test (FAT) and FPGA-assisted programming (FAP) they provide enormous flexibility for adaptation to individual test and measurement requirements. Chip-embedded instruments have been utilized for years in chip test, for example in form of built-in self-test (BIST) IP. However, access to these instruments has not been standardized in the past, something that will be changed with the new IEEE P1687 (also known as IJTAG). One of the leading system technologies for the holistic support of chip-embedded instruments is known as ChipVORX. The important area of device programming, too, benefits from a number of different ESA technologies. By utilizing primarily the same infrastructure as the previously discussed test solutions, a high degree of synergy between test and programming applications can be obtained.

In-system-programming (ISP) is a collective term for the programming of flash devices via boundary-scan and for the programming of PLD/FPGA devices through their test access port (TAP) and built-in programming registers, while the devices are mounted on the printed circuit board. For in-system programming of PLD/FGPA, special standards exist, such as IEEE Std 1532, JESD-71, and an industrial standard called serial vector format (SVF).

The premise of the core-assisted programming (CAP) strategy is similar to processor emulation test. The processor is controlled through its native debug interface in a way that allows flash or FPGA (design permitting) connected to the system bus to be erased, programmed, and verified. In the case of flash it does not matter whether it is integrated in the processor/microcontroller unit (on-chip flash) or connected as an external, discrete flash device or devices. Furthermore, it is possible to load only the flash handler/programming engine via JTAG into the processor and to download the flash data image through a high-speed communication interface on the processor CAP technology, such as VarioTAP, providing much higher in-system programming speed than boundary-scan based device programming.

One of the most interesting technologies for flash ISP, referred to as FPGA-assisted programming (FAP), is based on FPGA-embedded instruments. The embedded instrument in this case is a programming engine (programmer) soft macro, typically provided by a tool vendor and temporarily downloaded into the FPGA. Depending on the architecture of the programmer IP and the performance of the external control system, drastic improvements in programming speed compared to boundary-scan based ISP are possible. Meanwhile even universal, synthesis free solutions exist for FAP, such as those provided by ChipVORX.

The last access technology in this discussion is referred to as system level JTAG. While remote control through an external controller is possible, this technique typically employs a central test control unit integrated directly into the system design. Test vectors are usually stored locally on the system and a separate IC is commonly used as the test bus controller (although there is also the possibility to integrate the test bus controller function in an IC that also performs other functions in the system design). As the name implies, this method can be employed not only for individual boards but also for systems comprising multiple boards and modules.

The transition from traditional invasive test access and techniques to embedded system access is not a marginal change in the handling of test and programming vectors but rather a fundamental technological metamorphosis. Characteristics of these changes include: integration of test electronics in the system under test, inseparable coupling of functional and test circuitry in the system design, forming of partitioned test centres with various features, significantly wider range of test and programming strategies, possible utilization throughout the entire product life cycle, flexibility of reconfigurable pin-electronics with FPGAs, and availability of completely new instrumentation platforms. In practice, embedded system access represents in principle a transformation from a purely functional design into a functional design with integrated test capabilities, a combination of unit under test and tester, so to speak. Depending on the actual implementation of embedded system access, a wide variety of applications is possible. Currently, FPGA-based test in particular is a technology driver for progressively more complex test and measurement functions.

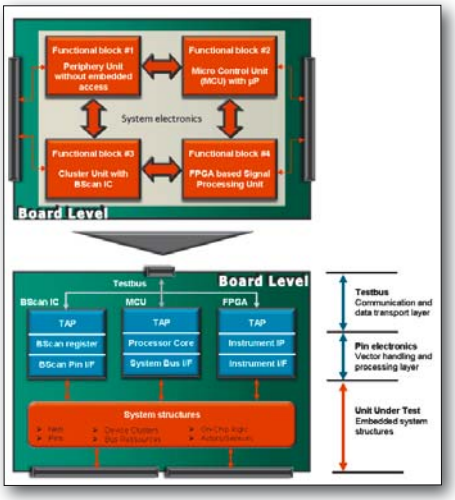


Figure 4. Transformation caused by embedded system access

This includes applications such as: voltage measurements, frequency measurements, temperature measurements, bit error rate tests (BERT) for high-speed signals, event counters, logic scopes, and many more. As a result, extensive design validation is possible in the lab or even at the designer's desk through one central communications and control channel. One big advantage of this methodology is that signals are accessible and measurements are taken directly inside the circuitry, avoiding artificial interference and distortion caused by mechanical probes, cables, and additional electrical loads, for example. With ESA the test and measurement results are not only more accurate but also more reproducible. Of course, for an efficient application of ESA techniques respective external instrumentation is needed.

So far we have primarily talked about the JTAG interface as the test bus. However, there are also a number of proprietary bus interfaces used in the industry, in particular for debug interfaces on processors, such as serial wire debug (SWD), spy-bi-wire (SBW), or background debug mode (BDM). For ATE vendors this means that their test bus controllers need to provide the required flexibility to support any of such interfaces; even a mix of different test bus interfaces in multi-processor applications should be supported. Furthermore, the various ESA technologies must be supported by powerful software tools and must be made available to the user in intuitive graphical user interfaces. In this context we need to consider not only the independent use of individual ESA methods, but also the potentially interactive application of various ESA technologies in order to gain extra benefits (such as improved fault coverage, for example).

This last requirement leads directly to another important topic: the combination of embedded system access with other access technologies, such as invasive board access (IBA) and native connector access (NCA), allowing embedded system access to be migrated into already existing test systems. In order to support this level of interactivity, ESA test equipment needs to provide very good integration features and must be available for all important integration platforms. Functional test in particular will play an important role, considering the continued rise of very powerful and open test and measurement platforms (such as PXI).

In the end, the transition to embedded system access with all its facets requires a completely new class of JTAG/boundary-scan instrumentation, putting enormous pressure on ATE vendors. First solutions are available in form of multi-dimensional JTAG/boundary-scan platforms. The term multi-dimensional reflects the support of the various dimensions and complexities of parameters, structures, functions, interactions, applications, and access technologies that come with embedded system access. One of the first multi-dimensional JTAG/boundary-scan instrumentation platforms is based on Scanflex hardware and System Cascon software. ■

System suppliers keep a watchful eye on signal integrity

By Tim Caffee, Asset InterTech

As system suppliers concentrate greater scrutiny on the integrity of signals on high-speed buses, the limitations of the instruments used to measure it, oscilloscopes and logic analyzers, come to light. Fortunately the versatility, agility and precision of embedded instrumentation are providing viable solutions for the validation of high-speed embedded systems.

■ Even the fastest, most advanced processors and other types of devices are no guarantee of high-performing systems. System throughput can grind to unacceptably low levels when high-speed chip-to-chip, input/output (I/O) and memory buses begin to choke because of poor signal integrity. And don't think that simply deploying the fastest possible buses will eliminate the problem. All too often, theoretical

bus speed is inversely related to the ease with which a bus can be coaxed into operating at its full potential. The higher the theoretical bus speed, the harder it is to achieve that speed and maintain it. In the final analysis, if system suppliers want to optimize system performance they must come to terms with validating signal integrity at every phase of the life cycle, beginning with design, moving into production, and continuing to field service.

For many years, engineers have relied on eye diagrams to give them a snapshot of signal integrity on high-speed buses. Unfortunately, the higher transfer rates on each successive generation of high-speed buses nowadays such as PCI Express I/II/III, the DDR1/2/3 memory bus, Serial ATA I/II/III, USB 1/2/3, Intel QuickPath Interconnect (Intel QPI) and others are causing eye diagrams to shrink, indicating a reduced margin for error for the signaling. This, in turn, has a direct effect on bus throughput, since slimmer operating margins, by defi-

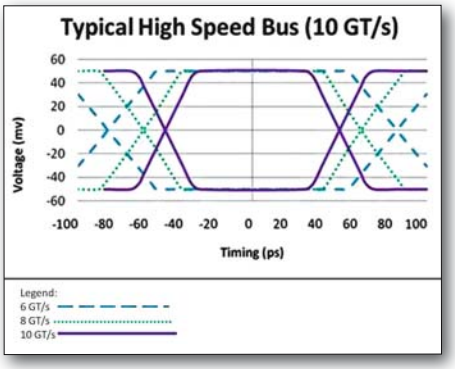


Figure 1. The eye diagram closes with each successive generation of a high-speed bus.

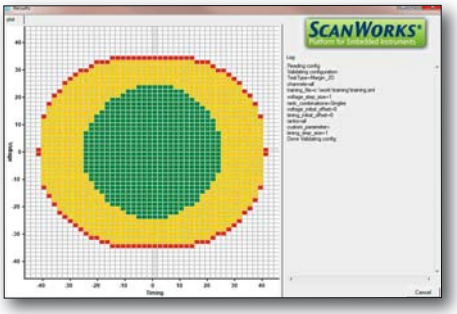


Figure 2. The screen capture shows an eye diagram generated from instrumentation embedded in silicon.

nition, lead to more errors, which slows bus traffic. Exacerbating the problem is the question of the adequacy – or inadequacy – of the instruments that typically generate the eye diagrams, such as oscilloscopes, and the equipment that tests circuit boards in production, like in-circuit test (ICT) systems.

To illustrate the problem of closing eye diagrams, consider three generations of a hypothetical high-speed bus whose theoretical transfer rate increases from six to eight and eventually to ten gigatransfers per second (GT/s). Figure 1 superimposes the eye diagram for each transfer rate on the same eye diagram. As the frequency of the signaling increases to achieve a higher transfer rate, the eye diagram becomes smaller, indicating smaller acceptable operating margins in terms of voltage and timing. Less room for error means that bus performance can be adversely affected to a greater degree by smaller amounts of jitter, attenuation in signaling voltage levels and variations in the manufacturing process. In other words, fewer or smaller anomalies can cause more distortion in the signaling, which degrades bus performance.

A closer look at timing issues demonstrates this point. At six GT/s, the first-generation of this bus has a fairly wide open eye diagram across the X axis where timing is plotted. The width of the eye measures is approximately 166 picoseconds (ps). In the next generation of the bus, where the frequency has increased to achieve a transfer speed of eight GT/s, the eye width has shrunk to 125 ps for a 25 percent reduction in operating margins. Lastly, the third generation of the bus increases its signal frequency again to achieve a 10 GT/s transfer rate. At this speed, the width of the eye diagram is reduced again to around 100 ps for another 20 percent reduction. While these two reductions in eye size may seem incremental, the total erosion of operating margins in the space of three generations of bus technology – probably over the course of two to five years – comes to a very significant 40 percent, or almost half of the operating margin.

In addition to timing anomalies, other factors can disrupt signal integrity, such as jitter or noise on the line, the attenuation of the voltage levels between transmitters and receivers, as well as variations in manufacturing processes at both the chip and circuit board levels. Moreover, on-board variations in voltage regulation and fluctuations in system-level operating temperatures can have profound effects on signal integrity.

At a time when system suppliers are concentrating greater scrutiny on the integrity of signals on high-speed buses, the limitations of the very instruments that have historically measured that signal integrity – the oscilloscopes and logic analyzers – have come to light. The same factor that raised signal integrity as a critical issue – constantly increasing demands for higher system throughput – is causing problems for measurements generated by probe-based instruments like oscilloscopes in design and field services, as well as ICT systems, flying probe testers and manufacturing defect analyzers in manufacturing.

The problems stem from the capacitive coupling effects probes have on very sensitive high-speed buses with smaller and smaller operating margins. Probing a bus will introduce distortions into the signal. In fact, placing a test pad on a bus to provide access to a probe will also cause anomalies. As a result, nowadays best design practices typically prohibit test pads on these sensitive buses. That would rule out validation with a probe-based instrument, but even when probe access is available, only expensive, high-end scopes capable of higher order mathematics are able to measure signal integrity because these scopes must be able to recover or de-embed the unadulterated signal from the observed signal, because the signal observed by the scope will include the distortions introduced by the probe itself.

Fortunately there is a more economical and straightforward way to generate empirical signal integrity data. Various validation, test and debug instruments are now being embed-

ded into silicon. Some can observe the integrity of bus signaling as well as perform other test functions. This embedded instrumentation is typically accessed by way of standard technologies, such as the IEEE 1149.1 boundary-scan (JTAG) test access port (TAP) which is present on practically all processors and many other types of devices. JTAG provides access to an external software-based platform that can manage the embedded instruments in the system as well as compile and analyze their test and measurement results.

Given the critical nature of bus performance as it relates to system throughput, validating the signal integrity of high-speed buses during all phases of a system life cycle is rapidly becoming a requirement, although different types of validation tests are deployed during each of the different phases of the life cycle. Even though the requirements of a particular phase will dictate the kind of validation routines performed at that point, the common denominator for each type of validation is quickly becoming non-intrusive embedded instrumentation.

For example, during the design phase when first prototypes of circuit boards have been assembled, bus performance must be validated to ensure the design meets the performance requirements of its specification. This will necessitate tests from many different perspectives and the collection of a significant amount of data to ensure that the prototypes perform to the design specs before it is released to production. Unlike functional test methods, embedded instruments can validate the high-speed buses of a design before the integration of firmware or an operating system. As a result, software development can continue independently of this board bring-up process.

During manufacturing, buses must be validated to ensure that variations in manufacturing processes have not degraded bus performance. Here, because test times must be short so that the beat rate of the production line will be maintained, a simple four-point margin test is sufficient to ensure the buses are operating effectively and at maximum speed. And finally, with systems in the field, validation will be a key diagnostic tool for identifying the root causes of poor system throughput. At this point in the life cycle, the time it takes a test to execute will not be as critical as determining the root causes of faults and failures, and identifying an efficient way to correct problems. Moreover, the particular troubleshooting algorithms employed will be driven by the characteristics of the failure. ■

Product News

Rohde & Schwarz: high-end signal and spectrum analyzer for microwave range

Rohde & Schwarz now offers a new R&S FSW signal and spectrum analyzer model for microwave applications up to 43.5 GHz. Harmonic mixers from Rohde & Schwarz extend the frequency range to 110 GHz. Developers of wireless, radar and satellite applications will appreciate the outstanding RF performance of the R&S FSW43.

News ID 16370

Wurldtech: robustness testing at all stages of product development lifecycle

Wurldtech Security released its Achilles Test Software, the software version of its Achilles Test Platform, extending its Achilles Test family of cyber security testing products to development teams of mission critical embedded devices. Achilles Test Software delivers the tools that development teams require to test critical software early in the development cycle, before they enter the QA lab.

News ID 16102

Renesas Electronics introduces new DSP library for RX MCUs

Renesas Electronics announced a robust DSP Library that improves ease of use and helps speed the implementation of DSC designs for developers working with Renesas' RX600 and RX200 series of microcontrollers. The new DSP Library provides a robust set of fully optimized and debugged functions that allow faster implementation of many of the numerical, filter and transform operations needed in a variety of consumer and industrial applications, including those for medical, building automation, industrial automation, sensing and audio.

News ID 16353

Green Hills: tools for AppliedMicro's new gen PacketPro2 processors

Green Hills announced its collaboration with AppliedMicro for the development of solutions for AppliedMicro's PacketPro2 family of single and multicore secure processors for enterprise networking, control plane and industrial applications. Green Hills Software's MULTI multicore debugger, optimising compiler, and processor probes will target the Keelback and Black Mamba PacketPro2 processors.

News ID 16116

PolyCore: Poly-Platform 2.0 now available for TI TMS320C6678

PolyCore Software announced that Version 2.0 of its Poly-Platform multicore software platform is available for Texas Instruments' TMS320C6678 digital signal processor, based on the KeyStone multicore architecture. Poly-Platform is a bundle of productivity tools and runtime communications engine that simplifies the process of migrating to and developing applications for multicore platforms.

News ID 16351

LDRA integrates tool suite with IBM Rational Rhapsody

LDRA has fully integrated the LDRA tool suite with IBM Rational Rhapsody ensuring a seamless workflow from model-driven development to test and verification. IBM Rational Rhapsody, a UML-based modeling and code-generation tool, speeds the design of complex systems that often must meet industry certification standards. The LDRA tool suite intelligently obtains information from the model and automates the development and configuration of the potentially complex test harness.

News ID 16350

PragmaDev: latest version of ITU-T SDL standard to support C language

The International Telecommunication Union has officially standardized the support of the C language as a possible action language in SDL (Specification and Description Language).This initiative started by PragmaDev a decade ago has reached its conclusion the 16th of October 2012 when Appendix C of the Z.104 that describes the data types and action language of SDL modeling language has been adopted. PragmaDev team is very proud that its initiative around SDL-RT started in 2001 has finally turned out in a standardized extension of the language. The SDL language (Specification and Description Language) has been re-organized since its 2010 version.

News ID 16341

CMX: embedded software suite for STM32 family

CMX Systems offers two RTOSes, two TCP/IP stacks, five Flash File Systems and USB support for the STM32 processor families, which include STM32F1xx, F2xx and F4xx. Support is also provided for many compiler tool chains including ARM, GNU, IAR, KEIL, Rowley and Atollic. CMX-RTX is a truly preemptive, multi-tasking RTOS offering one of the smallest footprints, fastest context switching, and lowest interrupt latency times available on the market today. RTOS functionality provided in CMX-RTX includes: task, message, queue, system, event, memory, resource, semaphore, and timer management. CMX-RTX includes an intuitive Windows GUI which simplifies RTOS configuration.

News ID 16257

Cheap, fast and low power

Jim Stuart, Industrial MCU Marketing Manager EMEA, Freescale

Our industrial customers challenge us to provide solutions that allow system cost reduction, faster time to market, extended power efficiency, increased wired and wireless connectivity and easier-to-qualify functional safety solutions. Building on the sweeping success of the Kinetis K family launched two years ago at Electronica 2010 we have been following this up with several extensions to our portfolio of ARM-based solutions, which is a trend in itself. The demand for increased energy efficiency and extended battery life has been satisfied with the Kinetis L family which went to mass production on 25 September. It is the first low-cost 32-bit Cortex M0+ microcontroller to be brought to market, setting new standards for power efficiency (sub 50µA/MHz) as well as hitting a distribution price point of only 49 US cents for 10k units (satisfying a sub-trend to migrate away from 8-bit to 32-bit solutions). The Kinetis KW20 Wireless MCU has increased wireless connectivity capability, it integrates a class-leading RF transceiver, Cortex-M4 and a robust feature set for reliable, secure and low-power IEEE 802.15.4 wireless solutions. The Kinetis W series is optimized for wireless, providing the right mix of performance, integration, connectivity and security. The increasing complexity and demands of embedded industrial systems also create greater need for sophisticated human-machine interfaces (HMI) and multiple connectivity options with safe, secure and predictable operation. To concurrently provide rich HMI and real-time control means bringing together two very different system paradigms. For example, HMI computation focuses on efficiently processing pixels and displaying them on a screen, while guaranteed determinism requires highly predictable response times for tasks. Vybrid devices have a dual core architecture that combines the ARM Cortex-A5 application processor and the ARM Cortex-M4 for real-time control. The Vybrid portfolio is designed to be a transitional product from Kinetis MCUs featuring the ARM Cortex-M4 core and the i.MX 6 series featuring the ARM Cortex-A9 core, while also providing scalable devices that can address the needs of a market that demands critical safety and security, connectivity and rich HMI in the same piece of silicon. The Vybrid roadmap is built with this scalability and code compatibility in mind, so that the performance of the device roadmap grows with the needs of the customers long into the future.

The Freescale solution for functional safety, the PXS family of 32-bit power architecture dual-core microcontrollers targets industrial applications which require compliance with the IEC61508 (SIL3) safety standard. It reduces design complexity and component count by putting key functional safety features on a single chip with a dual core, dual-issue architecture, which can be statically switched between lockstep mode (redundant processing and calculations) to decoupled parallel mode (independent core operation). The performance of the PXS family is rarely experienced in a microcontroller, with over 600 DMIPS possible. ■

Automotive electronics trends

Ross McQuat, Automotive MCUs, Operations Manager EMEA, Freescale

In over 30 years of supplying the automotive industry with market leading microcontrollers, Freescale has seen many changes, from our first 8-bit controller with 20,000 transistors, to our latest Qorivva multi-core processors with over 200 million transistors. In this time we've witnessed the dramatic increase in processor speeds, ever more efficient power schemes, and an explosion in software complexity and the memory systems required to manage it. Despite all these changes though, some things remain constant, and that is our customer demand for ever greater levels of integration, more capacity for data communication, and the continued pursuit of safer vehicles. Integration of previously discrete digital functions and low voltage analog functionality is routine, but with space constraints on vehicle applications like window lift, gauges and HVAC motor control becoming ever more demanding, a new approach was needed. Freescale S12 MagniV portfolio simplifies system design in these applications with expertly integrated mixed-signal devices. With up to 128kB of integrated flash memory, easy-to-use S12 16-bit core and 40V analog capability, the MagniV family offers the right blend of digital programmability and high-precision analog, plus a portfolio of scalable memory options. Freescale has long been at the forefront of developing communications protocols, from our early adoption of the now ubiquitous CAN protocol, to currently driving the introduction of Ethernet connectivity in the automotive arena. By taking advantage of the MPC5604E utilisation of twisted-pair Ethernet connections, car makers can reduce material expenses and lower weight while improving performance. The MPC5604E compresses video data and transmits in real time via Ethernet, providing a low cost alternative to screened LVDS cabling. Freescale also provides an Ethernet streaming stack (software) so that customers can take full advantage of the hardware on the chip. The automotive industry has relentlessly pursued safety throughout the age of electronic control, and this has recently been codified in the ISO26262 standard which describes the criteria which an automotive system or component must satisfy to be considered for use in safety-related systems. Qorivva MPC5643L 32-bit MCU was recently certified to the highest level of this standard making it the first semiconductor product to achieve the certification. This MCU built on Power Architecture technology, is designed for use in a wide range of automotive applications that require high levels of automotive safety integrity. ■

Trends on the horizon

Krunali Patel, General Manager MCU Marketing and Systems, Texas Instruments

Three distinct trends are driving the overall growth in TAM for microcontrollers.

First: We, as consumers, are looking to add more functionality in our lives through smarter gadgets. We are more conscious than ever of the need to make the world green and to conserve resources for generations to come. And above all, we want to live longer. We are enabling a world of smart living with exciting evolutions in various ecosystems. For example, obesity is on an alarming rise. Consumers are now looking for preventative vs diagnostics capabilities in medical devices. The same is true for insurance providers and employers to help reduce overall cost of health benefits. A blood glucose meter, once typically used by diabetic patients, is now being transformed into a preventative, non-invasive gadget to help monitor blood glucose levels and modulate food intake, to prevent diabetes. With evolution of smart phones, cloud computing and a myriad of smart phone applications, data from such devices is now available to physicians for continuous monitoring.

Second: Microcontrollers have become complex to enable smart living. The evolution of deep submicron silicon technologies makes it possible to increase functionality without increasing silicon area, process node after node. The combination of technologies like high performance data converters, sensors, human interface technologies (e.g., touch and proximity

detection) and wireless communication protocols (e.g., NFC and WiFi) can be successfully re-used across consumer, industrial and automotive applications in the smart living world. With this convergence of technologies, microcontrollers have significantly evolved into intelligent and integrated devices. For example, smartphone-like touch interfaces are being implemented in industrial machinery touch panels, as well as in building automation applications like lighting control. Similarly, in automotive applications where microcontrollers may have been used traditionally in life-critical braking and airbag applications, they have found home in consumer-centric applications like remote keyless entry, car infotainment and safety applications such as advanced driver assistance systems and much more.

Third: System integration of complex microcontrollers that leads to higher overall functionality with increased simplification for end users is key to enable smarter living and growth of total available market share (TAM) for microcontroller penetration in everyday life. Our world is now full of inventors of all demographics, where Maker Faires lead to fascinating innovations/solutions with minimal investments. This world is a paradigm shift for semiconductor suppliers. Our customers look beyond silicon to differentiate their products. With their research and development time primarily spent on software and systems integration, they don't want to be concerned about transistor or circuit level details. TI offers a broad spectrum of microcontroller products for ultra low power, real-time control, safety, computing and connectivity applications. These are easy to use by customers with a strong ecosystem of software, tools, documentation and application notes. They provide a path to our customers to provide strong differentiation in their applications, bill of materials cost reduction by integrating needed analog for particular applications, as well as application-specific tools and software for ultra-low power uses, motor control applications, smart grid solutions, functional safety designs and more. In short, we are in the world of smart living that TI microcontrollers help enable. With as much transition and growth as microcontrollers have seen, I can't wait to see what's next on the horizon.

Product News

TI: wireless network processor offers three most popular ZigBee standards

Texas Instruments announced that the CC2538 ZigBee wireless network processor offers the three most popular ZigBee standards for one end-device (ZigBee Smart Energy, ZigBee Home Automation and ZigBee Light Link). Now a single end-equipment can support these three standards, offering a seamless user experience with fast switching between each standard making it seem like concurrent operation. In turn, manufacturers of smart meters, home appliances, home gateways and connected lighting products are able to deliver better quality of service.

News ID 16403

Freescale: Qorivva MCU receives ISO 26262 functional safety standard certification

Freescale Semiconductor is making it easier for automotive electronics suppliers to develop functionally safe systems in compliance with the ISO 26262 standard. The company announced the certification of its Qorivva MPC5643L 32-bit MCU by exida. The Qorivva MPC5643L 32-bit MCU, built on Power Architecture technology, is designed for use in a wide range of automotive applications that require high levels of automotive safety integrity, including electric power steering, active suspension, anti-lock braking systems and radar-based advanced driver assistance systems.

News ID 16112

ARM launches Cortex-A50 series of 64-bit processors

ARM announced the new ARM Cortex-A50 processor series based upon the ARMv8 architecture. The series initially includes the Cortex-A53 and Cortex-A57 processors and introduces a new, energy-efficient 64-bit processing technology, as well as extending existing 32-bit processing. The scalability of the processor series enables ARM partners to create SoCs that address diverse markets, from smartphones through to high-performance servers.

News ID 16374

The future of microcontrollers

Laurent Vera, EMEA Microcontroller Marketing Director, STMicroelectronics

ST strategy for microcontrollers is based on two product families. For the very low cost, we are focusing our efforts on the STM8, a very cost-effective 8-bit proprietary architecture. The STM8 product portfolio keeps on benefiting from a lot of innovation. We recently introduced STM8L and STM8S Value line. For the 8-bit market, innovations do not necessarily mean new features, higher memory range or higher CPU frequency. For STM8, the latest innovation lies in the cost reduction we have been able to reach to enable new markets in which microcontrollers were not considered before. We see more and more customers replacing simple logic, a combination of EEPROM with logic with the STM8. The 8-bit market and STM8 have a bright future, the vast majority of innovation will be coming from manufacturing efforts and supply chain optimization.

For the 16- and 32-bit market, we are investing massively on the STM32 platform. ST was the first major semiconductor company partnering with ARM to bring a Cortex-M 32-bit microcontroller on the market. Today, we have more than 350 commercial products in production, from a simple Cortex-M0, 20-pin package and 16 KB of flash up to a very high-end Cortex-M4-based machine running at 168MHz em-

bedding 1Mbyte of flash and 192Kbyte of SRAM. We are now developing the STM32 platform in several directions. The first direction is performance. STM32 was first introduced based on a Cortex-M3 CPU at 72 MHz, we are now in full production with a Cortex-M4 at 168MHz, and will keep on bringing more performances to the market. There is a strong demand for more memory, more MIPS, more integration, customers want alternatives to MPUs and DSPs. We intend to keep our leadership position in race for performances. The second direction in which we are investing a lot is the development of our ultra-low power portfolio. The STM32L product portfolio intended for battery-operated products with a need for long battery life is starting to gather a lot of momentum in the market. Developing an ultra-low power product is a very demanding task; one does not write the firmware for a low power platform as for a generic one, the firmware needs to be optimized. We see more and more customers, willing to break free from proprietary architectures in this market. Customers feel that once they have invested too many resources on a proprietary architecture, they are stuck. Cortex-M based machines are a very good alternative. STM32L is the leading platform in this market, and we will keep on developing the portfolio. As for the STM32 standard portfolio, we will develop the low power platform to the low end and to the higher level of performances.

Last but not least, we are now considering the development of the ecosystem as the most important factor to increase our market penetration. Time to market is essential. Customers are looking for solutions, ease of use. We already have many software bricks available on the STM32 platform, coming from partners, open source or even designed by ST. We are developing the tools to make the most of this vast ecosystem. ■

Product News

Fujitsu: two new MCU families based on ARM Cortex-M4 and Cortex-M0+

Fujitsu Semiconductor has launched the new FM4 Family of 32-bit general-purpose RISC microcontrollers based on the ARM Cortex-M4 processor core, as well as the new FM0+ family, which utilises the Cortex-M0+ core. Fujitsu plans to start releasing sample quantities of products in these new families in summer 2013. Combined with the current FM3 family of microcontrollers, the Cortex-M4, M3, and M0+ processor core product group will comprise a broad-based line-up of more than 700 different products, whose consistent architecture and flexibility will now be an even better fit for growing customer needs in the areas of higher performance and lower power consumption.

News ID 16407

Renesas: ARM-based MPU family for graphics, HMI and office networking

Renesas has disclosed details of its roadmap for next-generation microprocessors. The new family of ARM-based high-performance embedded MPUs will be called the "RZ family" and will be developed for applications requiring high-speed data processing in excess of 300 MHz, specifically Human Machine Interfaces and Networking. Across the embedded market space, two of the most important system developments are in terms of adding additional services through increased connectivity and ensuring that the end-user has a richer experience. This is focus area for the new MPU family from Renesas. The RZ family will include up to 10MB of internal RAM and has been designed to allow GUI and Networking development teams to not only achieve high performance but also reduce the bill of materials cost and lower the system power consumption.

News ID 16329

Toshiba: ARM Cortex-M3 MCU with USB device controller

The latest 32-bit ARM Cortex-M3 microcontroller from Toshiba Electronics Europe will reduce the component count of industrial and digital consumer applications where high performance, low power and USB functionality are key design requirements. The TMPM365 integrates the ARM Cortex-M3 core, a USB device controller, a 12-channel ADC, on-chip program and data memory, timers and configurable serial connectivity options into a BGA package measuring just 9 x 9mm.

News ID 16240

Industrial motor control demands precision speed and isolation

Aengus Murray, Motor and Power Control Applications Manager, Industrial and Instrumentation Segment, Analog Devices

Industrial automation companies need to continuously to improve the energy efficiency, dynamic response and precision of motor drive systems used in factories and processing plants, to reduce energy consumption and improve production throughput and quality. Emerging requirements now include advanced safety and network connectivity to improve operational efficiency and reliability. These performance improvements are all enabled by improvements in motor drive feedback signal acquisition and motor control signal processing, combined with communication interfaces and system control functions.

In an AC drive system power flows from the input line through the bridge rectifier to the DC link, the three-phase inverter, and finally to the AC motor. The inverter gate drive signals and motor current feedback signals must be isolated from the power circuits because of the high voltages present. Therefore high performance isolation technology is a key element in any motor drive system. A precise motor winding current signal is acquired using a shunt resistor connected to a ADC front end modulator. This simplifies the signal isolation task because the modulators' digital outputs are more easily isolated than analog signals. This approach is now the preferred methodology in AC servo drive systems, because it provides lower offset and better gain matching than isolation amplifiers or Hall effect current

sensors. Current feedback accuracy and converter dynamic performance is the key to delivering smooth torque at low speeds from an AC motor. Additionally, position and velocity feedback are signals acquired from sensors such as sine-cosine optical encoders or resolvers. Sampling the encoder analog output signals using a fast ADC delivers much finer precision than simply counting zero crossings. This is again the preferred approach in servo systems, but resolvers are still used in applications demanding more robustness. Integration of the servo drive in the automation system requires a torque, velocity or position command interface to the machine controller. Industrial network standards have advanced over the years from simple serial field busses to using modified high speed Ethernet. However, there is still a significant challenge in precisely synchronizing command signals in equipment such as machine tools or industrial robots. Because of this, an analog interface is still the preferred option in industrial equipment and 12-, 14- and even 16-bit precision converters typically provide this function. The industrial fieldbus or Ethernet connection is still required because manufacturing control systems still require connectivity to the drive to enable complete view into all layers of the manufacturing process. Many of the fieldbus standards such as Modbus, DeviceNet or CClink use standard interface ports such as CAN or UART, but the signals must be isolated from the network. The h/w interface is simplified by transceivers that integrate both the driver and isolation technology.

The core element in the drive system is the motor control processor or processors that implement the motor control algorithms and manage the system functions such as communication interfaces, drive configuration and the safety functions. Servo control systems often have more than one processing block to maximize control performance but regardless of the integration level, support of the motor control signal chain needs advanced 16-bit converter technology that can be integrated as needed with either high speed processors or high speed isolation technology such as iCoupler. ■

Product News

ams to roll out first ISO26262 automotive products

ams is approaching volume production of first automotive products developed along the new functional safety standard ISO26262. Released in 2011, the ISO26262 standard is the major global regulation governing functional safety in road vehicles. The vast majority of today's automotive ICs under development at ams include ISO26262 requirements. Device applications cover electric power steering, pedal and position sensors.

News ID 16273

Microchip expands low-power Op Amps into higher voltages

Microchip announces three new families of low-power, general-purpose operational amplifiers that expand the range to 12V supply voltages. Because the MCP6H7X/8X/9X maintain the same pin-outs and features as Microchip's existing 6V and 16V families, designers can easily migrate to the ideal voltage rail, in addition to the new families' higher-speed Gain Bandwidth Product range of 2.7-10 MHz.

News ID 16368

ams: NFC interface chip harvests energy from RF emissions

Implementing instant, high-speed Near Field Communication between two independent devices has been made easier and cheaper with the introduction of the AS3953 interface chip from ams. The AS3953 offers a high data-rate interface between a NFC device such as a smartphone and any host microcontroller with a standard Serial Peripheral Interface.

News ID 16398

Model-based design keeps the entire system in focus

Dr. Joachim Schlosser, Manager Application Engineering, MathWorks

The increasing functional complexity of devices, machines and plants makes the software used to control and monitor them even more essential. At the same time, there is growing pressure on developers to make innovative systems ready for the market even faster. However, the innovation process unleashed by new technologies is raising the level of sophistication. Designers have less and less time to deal with increasingly great volumes of data. Mountains of data and dependencies are not just the product of the growing number of components and subsystems that have to be harmonised with one another. What makes matters even more difficult is the fact that a wide range of disciplines have to be conjugated so that the overall system can function smoothly: mathematics and information science, engineering sciences, natural sciences and economics can only collectively lead to a solution.

The following example from the field of renewable energy generation clearly illustrates the problems associated with mutually dependent parameters. The electricity produced by a wind farm is not just contingent on the wind strength. What also counts is the capability of the turbine to turn into the wind - and to squeeze out just that little bit more energy through the positioning of the rotor blades. Background control mechanisms regulate the mechanical systems. The varying yield has to be processed by the inverter, which

prepares the electricity before it can be fed into the power grid. The more effectively these systems are coupled together, the lower the dissipation rate and the less risk there is of grid malfunctions. Last but not least, the onus is on the management experts who have to develop their price models based on a variable feed-in performance and plan the wind farm several years in advance.

The success of the system as a whole is dependent upon how well its component systems are harmonised with one another. To achieve this, engineers, machine builders, computer scientists and management experts have to sit down around the same table. Today, the convergence of these disciplines can no longer be mastered just with pen and paper, as the specialist departments involved also want to see what impact the individual design-related decisions will have on their respective working environments. Computer simulations are indispensable for developing an ideally aligned overall system. A standardised platform for bringing together all the needs of the disciplines participating in the development process forms the basis for a solution. The common denominator here is mathematics. It efficiently reconciles all the subsystems and disciplines with its algorithms and the aid of a suitable ecosystem of software tools.

Not only has industry recognised the significance of these design tools for model-based development. The trend at universities and other higher education institutions is towards project-based learning. Theory is very quickly tried out in practice to make sure that the engineers of tomorrow are fit to take on complex development tasks. They learn that design tools serve as effective development accelerators with which even complex overall systems can be set up. With the right tools, development times can be accelerated by up to a third, or correspondingly more can be achieved within the same time frame, thus satisfying the need for a fast and effective market launch. Mathematics gives a boost to make the development of products even faster - despite, or perhaps because of, the increasing complexity of the systems involved.

Product News

LDRA selects distributor Logic Technology to extend European sales

LDRA has appointed Logic Technology to extend LDRA's reach into the German- and Dutch-speaking regions of Europe for safety-, mission- and security-critical markets. With nearly 20 years' experience in embedded technology sales, Logic Technology brings engineering-savvy expertise to customer sales throughout Germany, Benelux, Austria and Switzerland.

News ID 16396

Agilent: new software for X-Series signal analyzers

Agilent Technologies releases new software for the X-Series signal analyzers offering expanded WLAN support to include the emerging 802.11ac standard. In addition to supporting 802.11a/b/g/n, the N9077A WLAN measurement application now offers one-button 802.11ac testing with a new option (4FP), enabling design verification and validation early in the product-development process.

News ID 16390

Tektronix: mixed domain oscilloscope gains worldwide industry recognition

Tektronix announces that the MDO4000 Mixed Domain Series oscilloscope has won two prestigious awards in France the "17th Palmarès technologique de Mesures 2012" award in the category of Instrumentation and the "15ème éditon des Electrons d'Or'" award in the instrumentation electroniques category. With these two new awards wins, the MDO4000 has been recognized globally with 12 prestigious industry awards.

News ID 16167

Instrumentation revisited

Rahman Jamal, Technical and Marketing Director Europe, National Instruments

It does not require the capabilities of a clairvoyant to recognize that fixed-functionality devices are becoming a relic of the past. The PDA, the portable music player, the map, and countless other tools are more and more being replaced by smartphones. Essentially, it all boils down to software that enables flexible computing platforms that can do so many things in one device and thus change its personality as required. But if you look at the basic model of instrumentation, it has remained largely unchanged. Engineers and scientists wanting to make measurements first purchase fixed-function hardware from test and measurement suppliers, and use software, such as NI LabVIEW, on a standard desktop PC to extend the hardware functionality with signal processing, decision making, automation, and so on.

Coming from the world of instrumentation, we at National Instruments coined the phrase "the software is the instrument" in the 1980s to describe the importance of software for automating multiple devices in the test systems you design. With the introduction of the NI LabVIEW system design software, National Instruments redefined the way engineers and scientists think about instrumentation. We have invested years in development to simplify the process of controlling instruments from multiple vendors through LabVIEW instrument drivers. By introducing a PXI vector signal transceiver (VST), we've given more power to the system designer to not only craft the system software around the instruments, but to design the software that runs within the instrument - hence, the world's first software-designed instrument. The NI PXIe-5644R

RF vector signal transceiver (VST), the first software-designed instrument, combines a vector signal generator and vector signal analyzer with a user-programmable FPGA into a single PXI modular instrument. Engineers can transform the vector signal transceiver into a new instrument or enhance its existing functionality using NI LabVIEW system design software. The new VST is ideal for testing the latest wireless and cellular standards such as 802.11ac and LTE. The new NI PXIe-5644R VST is designed to be smaller, lower cost, and more software-centric from the ground up. Based on industry-leading FPGA technology, and the principle of open-source software and firmware completely written in LabVIEW, the VST hardware design pushes software as close as possible to the point where RF is converted to bits. By replacing fixed, vendor-defined hardware with a flexible, software-designed approach, the VST empowers test engineers to design exactly the instrument functionality they need. LabVIEW software combined with this new class of RF instrumentation empowers any engineer or scientist with RF knowledge to successfully design new features or enhance existing ones within the instrument. The software should first give you a way to design the software in the instrument at a system level, simplifying the complexity of the instrument into basic blocks for visualization and programming. Then the software should abstract the complexity of the software and firmware of an RF instrument at a fundamental level, so that you can quickly understand the signal flow and know when and how to make additions and modifications. This helps you dig into each abstraction in a hierarchical way to access every function in the instrument. LabVIEW is uniquely suited to each of these requirements. It is equally adept at optimizing parallel programming for FPGAs on instruments, real-time processors, and software on the PC. The native dataflow programming model also provides an intuitive way to represent the movement of data from the I/O pin to your application. In this way, it helps solve the visualization problem and the implementation in the same diagram. For some, the applications and potential are obvious; others will take a while to embrace this new approach. It's similar to the advance of user-empowered smartphones. Looking back, you cannot imagine life without the diversity of applications solved through this single device, but when the first smartphone came to market, most of the world still viewed it as a simple telephone. How will your perceptions of instrumentation change once software-designed instruments become mainstream?

Product News

SEGGER: encryption now available for emFile embedded file system

SEGGER introduces encryption for its emFile embedded file system. This add-on provides an easy way to encrypt storage media either in its entirety, or on an individual file basis. The encryption layer may be used with both available file systems FAT and SEGGER's EFS, as well as on all supported storage types, such as NAND, NOR, SD-cards, MMC cards, CompactFlash cards, etc.

News ID 16246

Tektronix: Mixed Domain Oscilloscope series now with entry level models

Tektronix has expanded its MDO4000 Series of Mixed Domain Oscilloscopes to include two new entry level models. With the same features and functionality of the 12-time award-winning MDO4000, the new models put breakthrough time and frequency domain analysis in the hands of engineers at a more affordable price level.

News ID 16235

IAR: KickStart Kit for Fujitsu MB9BF618T

The KickStart Kit for Fujitsu MB9BF618T allows to design, develop, integrate and test applications and contains: MB9BF618T evaluation board from IAR Systems; IAR Embedded Workbench for ARM, 32KB Kickstart edition and 30-day full functional evaluation edition; IAR visualSTATE evaluation edition; IAR J-Link on-board and example applications for the board.

News ID 16295

United hard- and software development

Frank Krämer, Technical Marketing Director EMEA, Altium

■ Software is a fundamental part of developing electronic devices today. It's intimately related to the underlying hardware, yet traditional hardware design environments ignore its existence. At Altium we believe that software design should be a core element of the design system. Unlike conventional tool chains where software development and FPGA design are tackled using separate, disconnected applications, we've been focused on getting embedded hardware and software development inside a single design environment. Writing and debugging application software, implementing the code on programmable hardware and testing the combined result are all performed within one design system, without the need for complex exchanges of design data between applications.

Because Altium Designer employs a single model of the design data, any changes in the hardware domain will automatically propagate to the embedded design space. With this architecture in place as a backbone for our customers engineering environment, we use the unified data model to care for another urgent need in the engineering community: management of design data, which includes various design disciplines during the whole design process all the way through to manufacturing. Independent market surveys show that leading electronic design companies that have formally implemented workflows around data management, ECAD/MCAD integration, PCB/FPGA co-design or design re-use gain significant competitive advantages. Altium Designer lets us provide a unified tool to our customers, allowing them to implement out-of-the-box solutions in those areas and achieve their goals more successfully.

On the tool side, we see the strong need to provide efficient tools for tasks like sharing libraries between users, and to integrate version control for an auditable track of design changes. Tools and methodologies for design re-use from the very beginning are also very crucial, in order to enable repeatable and controllable design release and test processes to create error-free manufacturing data with no need to rely on emails back and forth.

Besides providing pure design functionality within the design tool, we will continue to create systems which help designers early in the design phase to make intelligent decisions when choosing the components for their design. Apart from the functionality of a device, there are different aspects which are equally important and might make the difference between a winning or losing product. Therefore information about lead time, availability, cost, second source, alternatives as well as design intelligence such as successful usage of a component/circuitry in former designs will be needed in the design environment.

Having these data early in the design process makes the design re-use much more efficient. We see different ways how such information can be provided. Web-based applications are of course very well suited to provide real-time supply chain information about components. This is why we extend both functionality and content in our online platform AltiumLive. Over the last couple of months for example we have been releasing more than 100,000 design-ready components - visible in AltiumLive and directly accessible from within the design environment so that they can be placed in a design project with a single mouse click - with all data needed to drive the project through to manufacturing. ■

ECE

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SYSGO strengthens presence in Turkey by partnering with G-TEK

To efficiently address new opportunities in the Turkish market, SYSGO is now partnering with G-TEK, a company providing software solutions, training, consulting and technical support to its customers. Nowadays, software is getting more important in embedded systems. G-TEK's added value relies on its capacity of providing high-quality solutions for real-time and embedded systems, performing software testing and guaranteeing security.

News ID 16270

IAR significantly improves development tools for Renesas MCUs

IAR Systems announced new user-friendly functionality in its development tools for Renesas' R32C and 78K microcontrollers. The updates include a new editor and source browser, which enables features such as auto-completion, code folding, block selection, block indentation, bracket matching, and zooming. The latest version of IAR Embedded Workbench for R32C also adds integration with the version control system Subversion.

News ID 16326

Digia joins forces with KDAB and ICS to host Qt Developer Days

Three of the leading players in the Qt ecosystem – Digia, ICS and KDAB – are joining forces to host Qt Developer Days 2012 in the US and Europe. As custodian of the Qt Project, Digia is committed to working with the Qt community to ensure the continuing development of open source and commercially licensed software in a manner that benefits all users. Used by over 450,000 developers worldwide, Qt is a full framework that enables the development of powerful, interactive and platform-independent applications.

News ID 16271

LDRA: tool verifies test coverage completeness

LDRA has released LDRAcover, a stand-alone code coverage tool that verifies the source code of an application has been fully structurally tested. This offering responds to the needs of companies that wish to improve overall quality of code by ensuring complete testing, as well as those companies that must meet the most stringent levels of code verification in markets such as avionics, defense, industrial controls, automotive and medical devices.

News ID 16163

QA Systems enhances testing tool for C/C++ embedded systems

QA Systems announces the general release of Cantata 6.2 - the latest version of the Cantata unit and integration testing tool for C/C++ embedded systems. Including more than 30 separate enhancements and over 40 fixes, Cantata 6.2 has been specifically developed to simplify, further automate and speed up the software testing procedure. Cantata 6.2 is now also available as a complete built-on Eclipse development environment or as a set of Eclipse-ready plug-ins supporting the last four Eclipse releases.

News ID 16315

Wind River adds Yocto Project to Auto IVI Software Platform

Wind River has added Yocto Project components into Wind River Platform for Infotainment. Using Wind River Platform for Infotainment, customers can quickly build a GENIVI-compliant automotive in-vehicle infotainment (IVI) platform based on the Yocto Project development infrastructure and take advantage of open source for its capability for rapid innovation.

News ID 16279

Enea: commercial grade Yocto based Linux distribution

Enea is announcing the first commercial release of the Yocto Project based Enea Linux v2.0 - a hardened, commercial grade Linux distribution addressing next generation communications and networking systems. Enea Linux v2.0 is the Linux distribution for communications and networking and includes a comprehensive cross-development tool chain and runtime environment with guaranteed performance and quality of service, flexible support offerings, worldwide support and maintenance, and expert professional services.

News ID 16221

Vector: AUTOSAR 4.0.3 basic software available

Vector has extended its AUTOSAR solution for AUTOSAR 4.0.3. This version supports automotive OEMs and suppliers in implementing the latest AUTOSAR standard. The solution consists of the MICROSAR basic software and the new generation of the DaVinci Configurator Pro configuration tool. Vector has acquired extensive experience in implementing MICROSAR basic software in over 200 production projects.

News ID 16188

Adeneo Embedded sets up engineering and sales office in Germany

Adeneo Embedded announces the creation of a new sales and engineering office in Frankfurt. This new operation will be the third full service engineering and sales office of Adeneo Embedded. With more than 60 engineers worldwide, and part of a 600 Employees' group, Adeneo Embedded provides a complete OS and Software expertise on Windows Embedded, Android and Linux technologies.

News ID 16089

IS2T: 28 Kbyte Java virtual machine supports 32-bit MCUs

IS2T has announced MicroEJ Java platform supporting the development and integration of Java-based functionality for low cost, memory-constrained, C and C++ applications running on Cortex M-based microcontrollers. MicroEJ provides a runtime Java platform that includes IS2T's MicroJvm, 28 Kbyte Java virtual machine, an optional RTOS (~10 Kbytes), all necessary libraries to run an advanced graphical human-machine interface (HMI), and a fully functional simulated platform that allows fully debugged and tested binary code to be ported directly to any supported MCU.

News ID 16389

Green Hills joins Xilinx Alliance Program

Green Hills Software has announced that it has joined the Xilinx Alliance Program as a Premier member. Green Hills' extensive support for Zynq-7000 devices ranges from the embedded multicore IDE, MULTI, to symmetrical multiprocessing support with INTEGRITY real-time operating system, to INTEGRITY Multivisor secure virtualization, and tightly integrated processor trace debugging via the Green Hills TimeMachine debugger and SuperTrace probe.

News ID 16386

EBV and Bridgelux sign distribution agreement for LED lighting products

EBV Elektronik and Bridgelux announce a distribution agreement to promote and deliver LED lighting products to customers within the EMEA region. Bridgelux actively supports its customers by delivering value-added, application-specific solutions that will open up new markets in solid-state lighting.

News ID 16399

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Tektronix: oscilloscope puts embedded system debug within easy reach

Tektronix introduced the MSO/DPO2000B series of oscilloscopes that put advanced debug features within easy reach of engineers and educators. The new oscilloscopes make it easier than ever for engineers – even those on very limited budgets – to gain all the debug advantages of full serial bus decoding and triggering. The 12-model MSO/DPO2000B Series oscilloscope features bandwidths from 70 MHz to 200 MHz. With industry-leading 1 M point record lengths, these oscilloscopes make it easy to find events of interest in long records using Tektronix' innovative Wave Inspector to perform manual or automated search.

News ID 16301

Granite: embedded motor control for electronic pipette

When Biohit set some really challenging targets to their upcoming new hand held servo motor controlled pipette, Picus, it was clear that a high tech partner in embedded motor controls was needed in order to meet the strict technical requirements in the given schedule. The main use of electronic pipettes is to speed up precision liquid dispensing and mixing in laboratories. Electronic pipettes are based on motor manipulated piston where strict safety and repeatability requirements set extreme challenges to the motor controller inside the device. Other major challenges are restrictions in physical size, weight, battery life as well as low BOM cost.

News ID 16323

Bluetechnix releases Argos smart camera series

Bluetechnix comes up with a new family of 2D and 3D smart cameras called Argos. Argos2D-A100 is the first product of this series, a standalone camera based on a Freescale i.MX535 ARM Cortex-A8 processor with 1 GHz. Provided with profuse 1 GB DDR2 RAM, the i.MX enables the user to run a full Linux kernel including GUI. This flexibility in terms of software is also given in terms of hardware. The design is developed totally modular to enable customers as well as developers to specify SoM, board, imager and optics separately whereas the case has not to be changed.

News ID 16281

Mouser introduces new RF technology site

Mouser Electronics announces its newest technology site on Mouser.com covering radio frequency (RF) Technology. The new site is designed to help design engineers find the latest RF product information by frequency range, plus access the latest technical resources in as few clicks as possible. The site features new products from industry-leading manufacturers such as Skyworks Solutions, M/A-COM Technology Solutions, TriQuint Semiconductor, and Texas Instruments, to name just a few.

News ID 16364

Optogan: scalable high-power LED module

Optogan has started mass production of its high-power X10 modules. Based on the innovative concept of scalability, flexibility and lean processing, the X10 modular Chip-on-Board solution significantly reduces the manufacturing costs of energy-efficient light sources based on LEDs. A unique feature of the X10 is a combination of small size, state-of-the-art module efficiency over 110lm/W, the optimal price and convenient size for mounting. Optogan has already produced modules consisting of 72 items that can be easily divided into LED elements of smaller sizes and power.

News ID 16318

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