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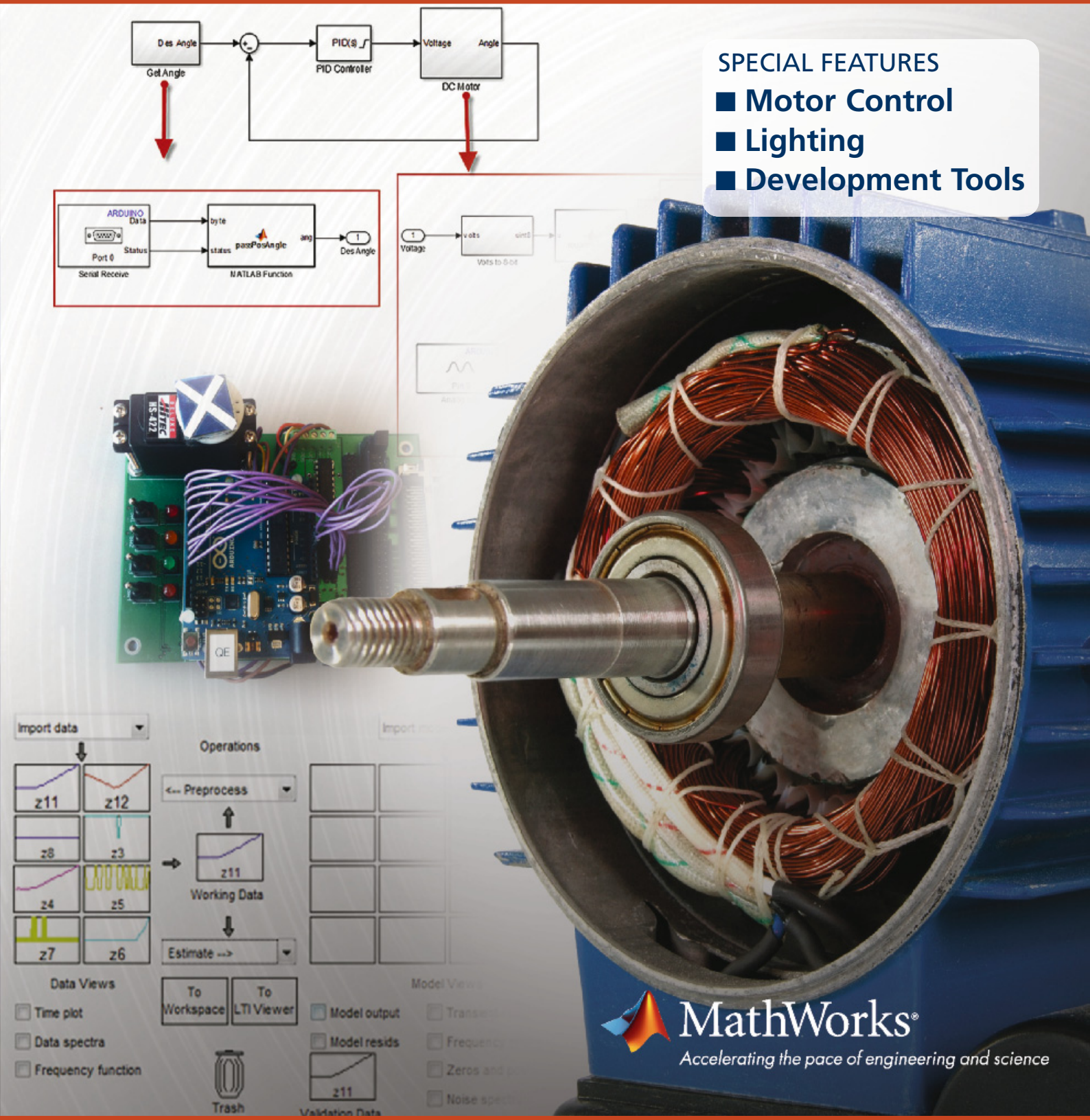
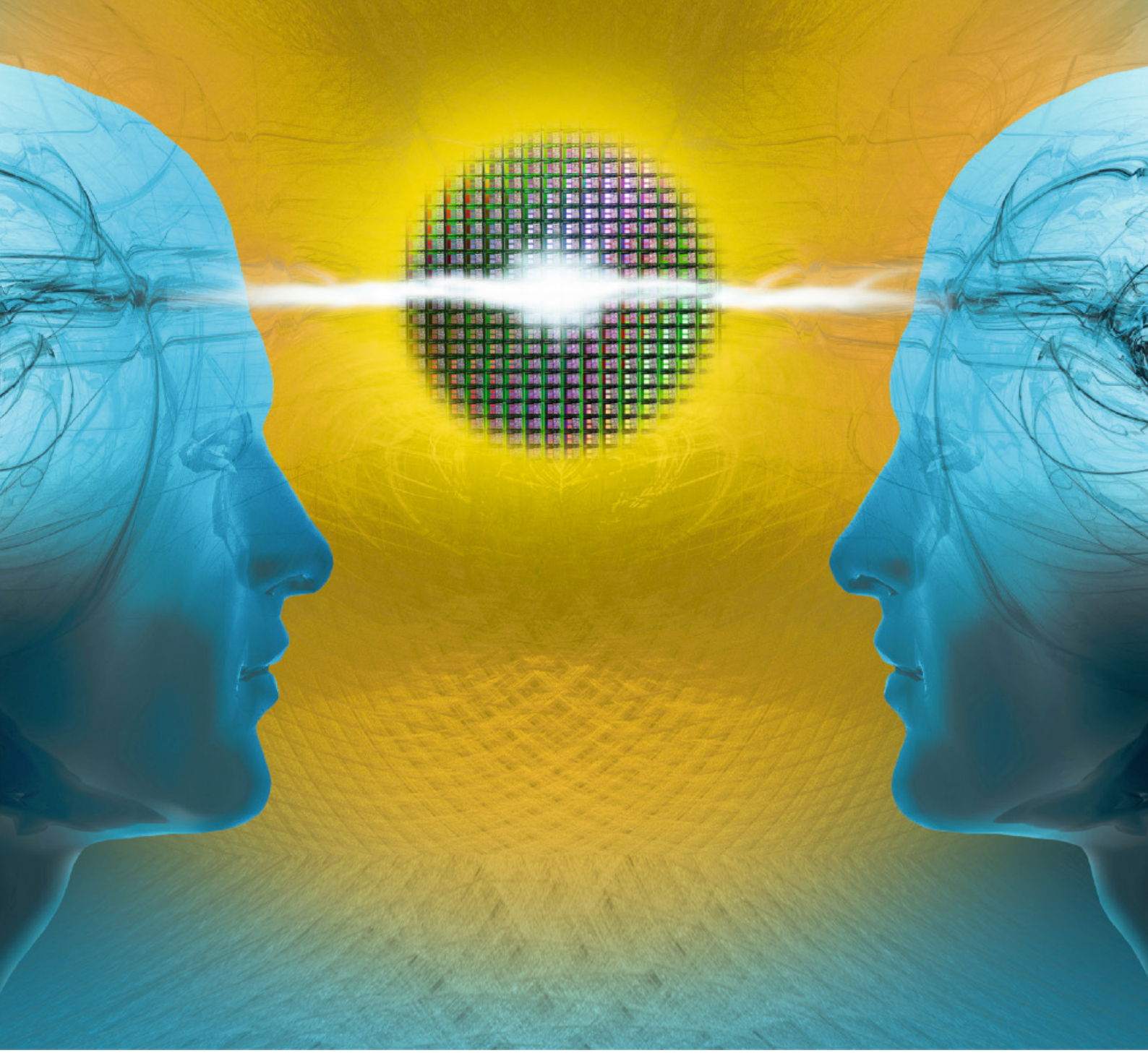


SPECIAL FEATURES

- Motor Control
- Lighting
- Development Tools

COVER STORY

Motor Control with Arduino: A Case Study in Data-Driven Modeling and Control Design



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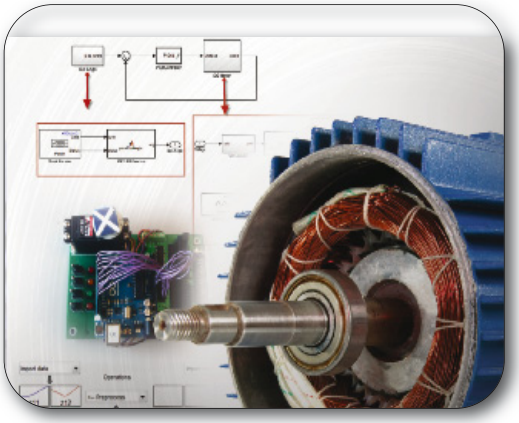
Motor Control with Arduino:

A Case Study in Data-Driven Modeling and Control Design

By Pravallika Vinnakota, MathWorks

Tuning a controller on a physical prototype or plant hardware can lead to unsafe operating conditions and damage the hardware. A more reliable approach is to build a plant model and simulate it to verify the controller at different operating conditions so as to run what-if scenarios without risk.



When first-principles modeling is not feasible, an alternative is to develop models from input-output measurements of the plant. A low-order, linear model might be sufficient for designing a basic controller. Detailed analysis and design of a higher-performance controller requires a higher-fidelity and possibly nonlinear model.

Using a simple control system for a DC motor as an example, this article shows how to identify a plant model from input-output data, use the identified model to design a controller, and implement it. The workflow includes the following steps: acquiring data, identifying linear and nonlinear plant models, designing and simulating feedback controllers, and implementing these controllers on an embedded microprocessor for real-time testing.

The DC Motor: Control Design Goals

The physical system is a DC motor connected to an Arduino® Uno board via a motor driver (Figure 1). We want to design a feedback controller for this motor to track a reference position. The controller will generate the appropriate voltage command based on the motor position reference data. When applied to the motor, this voltage will cause the motor to generate the torque that turns the motor shaft. We will use a potentiometer to measure the angle of rotation of the motor shaft, and feed this angle back to the controller.

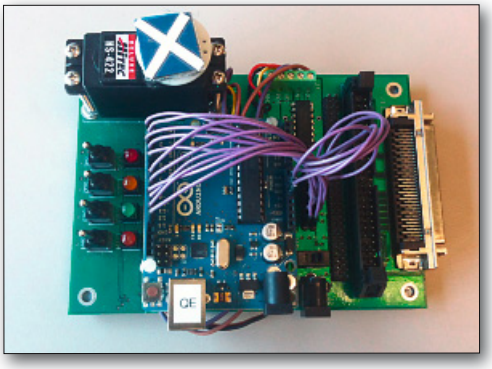


Figure 1. Arduino Board connected to the DC motor.

The motor driver integrated circuit (IC) increases the current capability and can drive the motor in both directions. We receive the motor position data through an Analog Input pin on the Arduino board and compute the error between the reference and actual data (the controller input). We send a voltage command (the controller output) to two Analog Output pins on the board as PWM signals. These signals are fed to the driver IC that provides the motor with the appropriate drive currents.

The controller must keep the system stable and provide fast reference tracking with minimal steady-state error and overshoot.

Acquiring and Processing Data

We connect the host PC to the Arduino board using a Simulink® capability that lets you generate an executable and run it on selected hardware. Figure 2 shows the Simulink library for use with Arduino hardware.

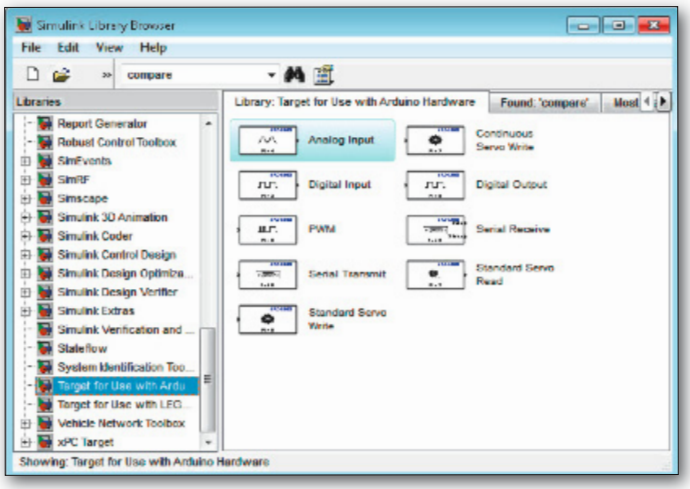


Figure 2. Target for use with Arduino hardware.

To collect the data, the Arduino board will send voltage commands to the motor and measure the resulting motor angles. We create a Simulink model to enable data collection. The host machine must communicate with the Arduino board to send voltage commands and receive back the angle data. We create a second model to enable this communication.

In the model that will run on the Arduino Uno board (Figure 3), the MATLAB® Function block Voltage Command To Pins reads from the serial port and routes the voltage commands to the appropriate pins. We use serial communication protocol to enable the host computer to communicate with the Arduino board. In the CreateMessage subsystem, a complete serial message is generated from the motor position data obtained from one of the analog input pins on the board.

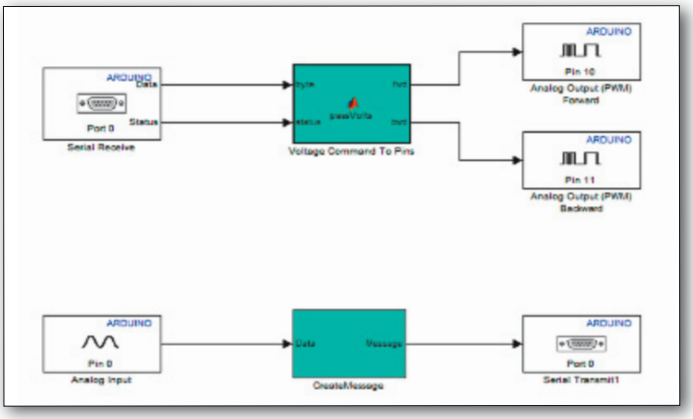


Figure 3. Simulink model that will run on the Arduino board.

We create a real-time application from the model by selecting Tools > Run on Target Hardware > Run. We are then ready to acquire the input/output data using the model that will run on the host computer (Figure 4).

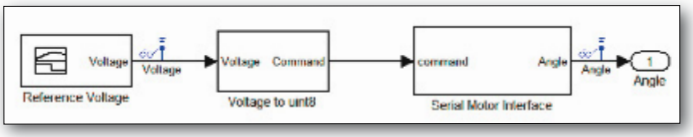


Figure 4. Model that will run on the host machine..

We send various voltage profiles to excite the system, and record and log the corresponding position data. At the end of the simulation, the signal logging feature in Simulink will create a Simulink data set object in the workspace containing all the logged signals as time-series objects.

Next, we prepare the collected data for estimation and validation. Using the following commands, we convert the data into iddata objects for import into the System Identification Tool in System Identification Toolbox™.

```
>> logsout
    logsout =
      Simulink.SimulationData.Dataset
      Package: Simulink.SimulationData
      Characteristics:
              Name: 'logsout'
       Total Elements: 2
      Elements:
       1: 'Voltage'
       2: 'Angle'
   -Use getElement to access elements by index or name.
     -Use addElement or setElement to add or modify elements.
     Methods, Superclasses
```

```
>> u = logsout.getElement(1).Values.Data;
>> y = logsout.getElement(2).Values.Data;

>> bounds1 =
iddata(y,u,0.01,'InputName','Voltage','OutputName','Angle',...
        ...'InputUnit','V','OutputUnit','deg')
        Time domain data set with 1001 samples.
        Sample time: 0.01 seconds
        Outputs      Unit (if specified)
          Angle      deg
        Inputs       Unit (if specified)
          Voltage    V
```

We will be working with 12 data sets. These data sets were selected to ensure adequate excitation of the system and to provide sufficient data for model validation.

Developing Plant Models from Experimental Data

Developing plant models using system identification techniques involves a tradeoff between model fidelity and modeling effort. The more accurate the model, the higher the cost in terms of effort and computational time. The goal is to find the simplest model that will adequately capture the dynamics of the system.

We follow the typical workflow for system identification: We start by estimating a simple linear system and then estimate a more detailed nonlinear model that is a more accurate representation of the motor and captures the nonlinear behavior. While a linear model might suffice for most controller design applications, a nonlinear model enables more accurate simulations of the system behavior and controller design over a range of operating points.

Linear System Identification

Using the iddata objects, we first estimate a linear dynamic model for the plant as a continuous-time transfer function. For this estimation, we specify the number of poles and zeros. System Identification Toolbox then automatically determines their locations to maximize the fit to the selected data sets.

We launch the System Identification Tool by executing
>> ident
We can import the data sets into the tool from the base workspace using the Import Data pull-down menu (Figure 5). We also have the option to preprocess the imported data. To start the estimation process, we select the working data that will be used to estimate a model and the validation data against which the estimated model will be tested. We can use the same data set for both estimation and validation initially, and then use other data sets to confirm our results. Figure 5 shows the System Identification Tool with the data set imported. The estimation data set, data set 11, comes from an experiment designed to avoid exciting nonlinearities in the system.

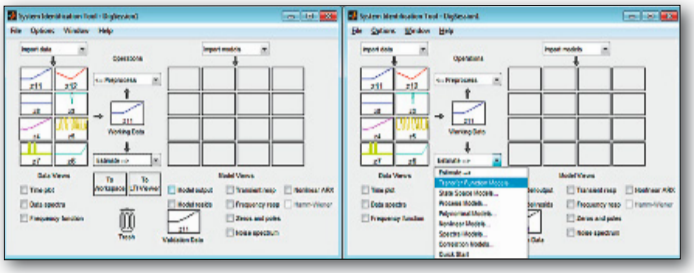


Figure 5. The System identification Tool with data imported.

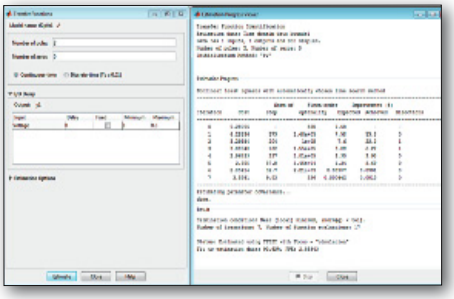


Figure 6. Continuous Transfer Function estimation GUI.

We can now estimate a continuous transfer function for this data. In our example, we estimate a 2-pole, no-zero, continuous-time transfer function (Figure 6).

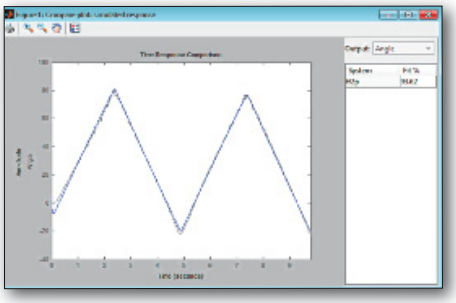


Figure 7. Plot comparing estimated model response and estimation data.

We compare the simulation response of the estimated model against measured data by checking the Model Output box in the System Identification Tool. The fit between the response of the estimated linear model and the estimation data is 93.62% (Figure 7).

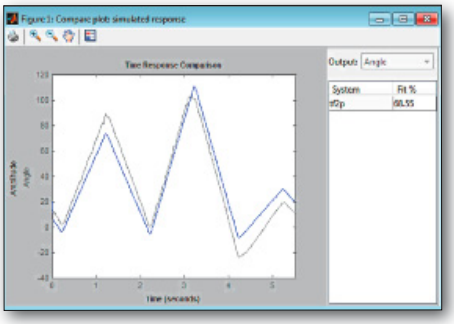


Figure 8. Plot comparing estimated model response with validation data.

To ensure that the estimated transfer function represents the motor dynamics, we must validate it against an independent data set. For this purpose we select data set 12, where the motor operates linearly as our validation data. We achieve a reasonably accurate fit (Figure 8).

While the fit is not perfect, the transfer function that we identified does a good job of capturing the dynamics of the system. We can use this transfer function to design a controller for the system.

We can also analyze the effect of plant uncertainty. Models obtained with System Identification Toolbox contain information not only about the nominal parameter values but also about parameter uncertainty encapsulated by the parameter covariance matrix. A measure of the reliability of the model, the computed uncertainty is influenced by external disturbances affecting the system, unmodeled dynamics, and the amount of collected data. We can visualize the uncertainty by plotting its effect on the model's response. For example, we can generate the Bode plot of the estimated transfer function showing 1 standard deviation confidence bound around the nominal response (Figure 9).

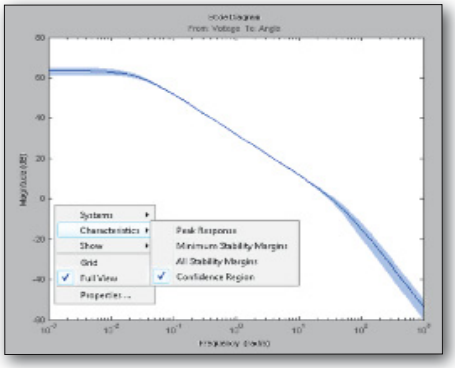


Figure 9. Bode plot of the estimated model showing model uncertainty.

Nonlinear System Identification

A linear model of the motor dynamics, created by using data collected from a linear region of its operation, is useful for designing an effective controller. However, this plant model cannot capture nonlinear behavior exhibited by the motor. For example, data set 2 shows that the motor's response saturates at about 100°, and data set 3 shows that the motor is not responsive to small command voltages, perhaps owing to dry friction.

In this step, we will create a higher-fidelity model of the DC motor. To do that, we estimate a nonlinear model for the DC motor. A closer inspection of the data reveals that the change in the slope of the response is not linearly related to the change in voltage. This trend suggests nonlinear, hysteresis-like behavior. Nonlinear ARX (NLARX) models offer considerable flexibility, enabling us to capture such behavior using a rich set of nonlinear functions, such as wavelets and sigmoid networks. Furthermore, these models let us incorporate what we have discovered about the system nonlinearities using custom regressors.

For the NLARX modeling to be effective, we need data that is rich in information about the nonlinearities. We merge three data sets to create the estimation data. We merge five other data sets to create a larger, multi-experiment, validation data set.

```
>> mergedD = merge(z7,z3,z6)
    Time domain data set containing 3 experiments.
    Experiment    Samples     Sample Time
      Exp1         5480         0.01
      Exp2          980         0.01
      Exp3          980         0.01

    Outputs      Unit (if specified)
      Angle        deg

    Inputs       Unit (if specified)
      Voltage      V
>> mergedV = merge(z1,z2,z4,z5,z8);
```

The nonlinear model had various adjustable components. We adjusted the model orders, delays, type of nonlinear function, and the number of units in the nonlinear function. We added regressors that represent saturation and dead-zone behavior. After several iterations, we chose a model structure that employed a sigmoid network with a parallel linear function and used a subset of regressors as its inputs. The parameters of this model were estimated to achieve the best possible simulation results (Figure 10).

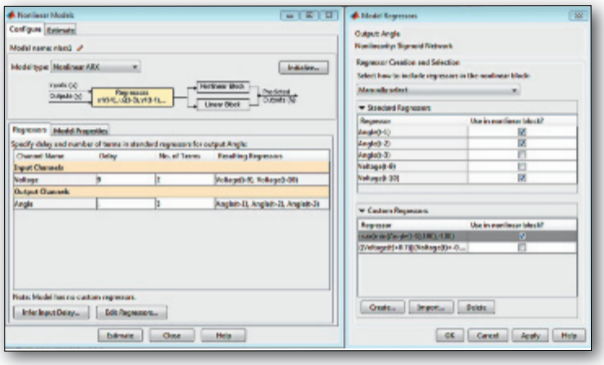


Figure 10. Nonlinear ARX model estimation GUI.

The resulting model has an excellent fit of >90% for the estimation data as well as for the validation data. This model can be used for controller design as well as for analysis and prediction.

Designing the Controller

We are now ready to design a PID controller for the higher-fidelity nonlinear model. We linearize the estimated nonlinear model at an operating point of interest and then design a controller for this linearized model.

We tune the PID controller and then select its parameters (Figure 11).

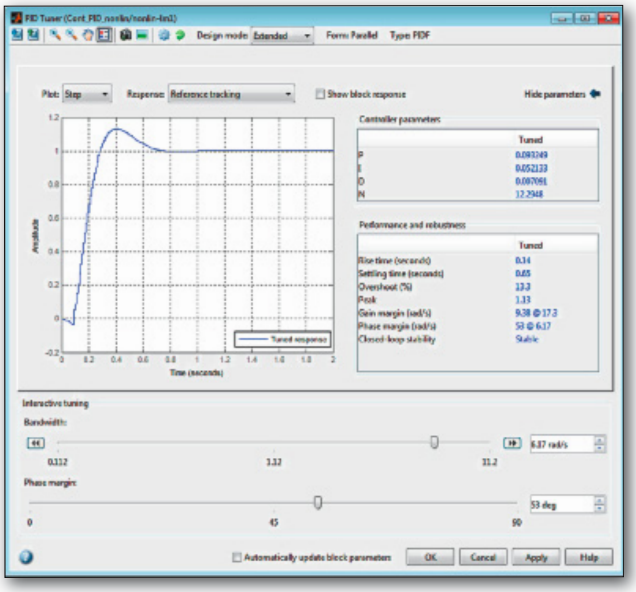


Figure 11. PID Tuner interface.

We also check how this controller performs on the nonlinear model. Figure 12 shows the Simulink model that we use to obtain the simulation response of the nonlinear ARX model.

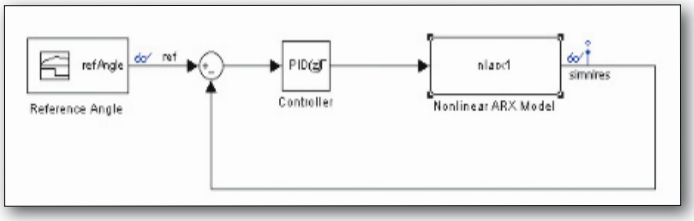


Figure 12. Simulink model for testing the controller on the estimated nonlinear model.

We then compare the linearized and nonlinear model closed-loop step responses for a desired reference position of 60° (Figure 13).

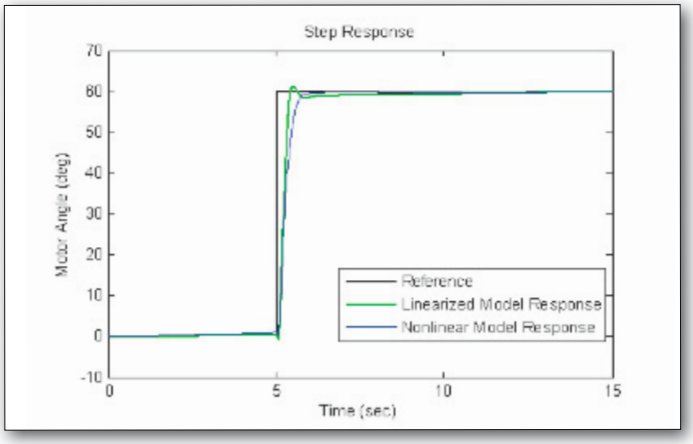


Figure 13. Step response plot comparing simulation responses of nonlinear and linearized models.

Testing the Controller on Hardware

We create a Simulink model with the controller and place it on the Arduino Uno board using Simulink built-in support for deploying models to target hardware (Figure 14).

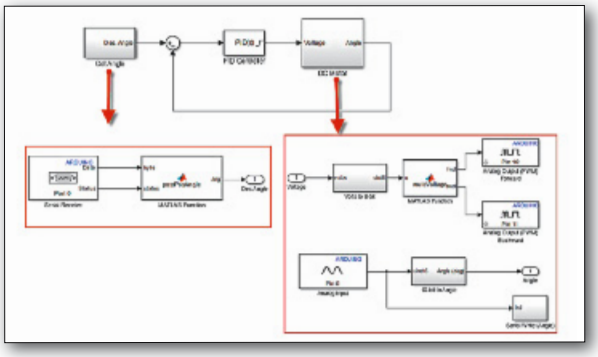


Figure 14. Model with the controller implemented on the Arduino board. The subsystem Get Angle receives the reference signal from the serial port and converts it to the desired angle of the motor. The DC Motor subsystem configures the Arduino board to interface with the physical motor.

We designed a controller by linearizing the estimated nonlinear ARX model about a certain operating point. The results for this controller show that the hardware response is quite close to the simulation results (Figure 15).

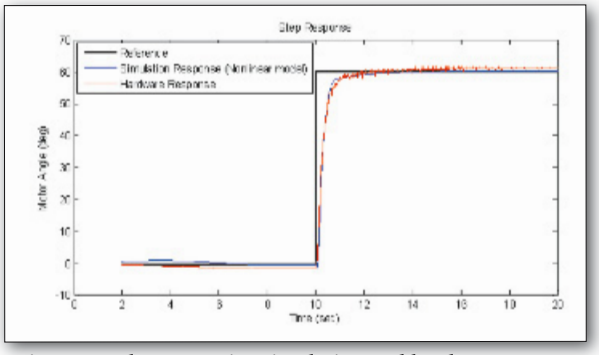


Figure 15. Plot comparing simulation and hardware responses to a step reference for a controller designed using a linearized model.

We also tested how well the controller tracks a random reference command. We see that the hardware tracking performance is also very close to that obtained during simulation (Figure 16).

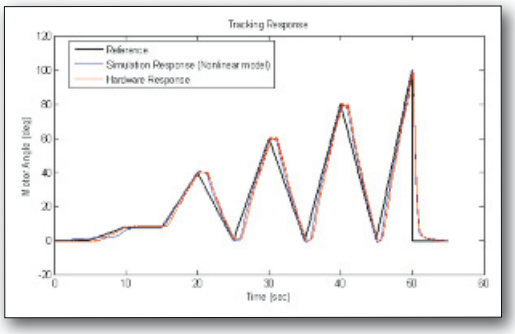


Figure 16. Plot comparing tracking performance in simulation and on hardware for the controller designed using an estimated nonlinear model.

This example, while simple, captures the essential steps for data-driven control. We collected input/output data from a given hardware target and used System Identification Toolbox to construct models of the system. We showed how you can create models of lower and higher fidelity and design controllers using these estimated models. We then verified the performance of our controllers on the actual hardware.

Validated methodology for designing safe industrial systems-on-a-chip

Safety has usually been added to systems by redundant controller or communication modules. These additional components incur higher costs and are less flexible and scalable than designing an application optimized for safety and cost-competitiveness from the start. This article exemplifies such an approach with a drive design.

When a company decides to develop a safe product, it must consider safety as core system functionality. Historically, safety has been added to the system by additional functionality such as redundant controller or communication modules combined with circuitry to monitor the system. These added-on safety components, introduced as an afterthought into the system concepts, incur significantly higher costs and are less flexible and scalable than designing a safe application, optimized for safety and cost-competitiveness, right from the start.

For a typical motor control application, such as a drive, the partitioning step separates the system into system control, communication, and real-time motor control functions. For example, the architect selects a software implementation for the control part and for the real-time portion of the system, and decides to use a hardware/software approach for the communications portion to support real-time Industrial Ethernet communication protocols. The next step is the component selection. The decision may lead to an implementation where the control software runs on a standard application processor, the real-time motor control portion will get implemented on a digital signal processor (DSP), and the communication within the system will be realized with an FPGA-based approach. An FPGA allows flexibility in the system to realize various different Industrial Ethernet standards like Ethernet/IP, EtherCat, Profinet, or Sercos III in the same device interchangeably. This flexibility for the communication part of the architecture allows for a standard hardware platform to be customized for the specific protocol needs of the end customer very easily.

After the partition has been decided and the components are selected, the design teams will work on the development of their part of the application independently. Then they will integrate the components to a full system, test the system functionality, and release the product. If the design is developed with functional safety as part of the product requirements, it is required to add additional phases to the project. To design a safe application with the goal to achieve functional safety certification, such as IEC 61508, the project complexity increases significantly to provide a clear and transparent project structure that matches the standard.

In the project startup and risk analysis phase, the scope for safety in the project is identified based on the general requirements for the application. The desired and achievable SIL for the application is determined, formulated, and documented for the implementation stages, and acts as the basis for the risk analysis and assessment. The risk analysis provides the foundation for measures that must be taken later in the process to develop a safe application. It represents the understanding of the product boundaries and is closely linked to the products scope definition. It provides the base for the required SIL, a detailed definition of the safety function, and the framework of the product documentation. This must happen on the component as well as on the system level. Following this step, the architecture for the application is developed to meet the functional requirements, as well as the safety requirements. The safety requirements are refined and the specific functions to be realized during operation and maintenance work are documented, together with the identification of strategies that must be followed to validate that the safety measures meet the requirements.

For a safe drive, the scope might include several aspects such as identifying whether the drive parameters are in the allowed range, or if a safety I/O signals a critical event. The most basic safety feature for drives is “safe torque off” (STO), in which the motor is disconnected from the power supply in a safe way. The procedure might also include communicating to the overall automation system that a safety event occurred and certain measures must be taken within a certain time window, such as a sequential shutdown of a whole application following a series of steps over a predetermined period of time.

The development of the validation plan might include methods of controlled failure insertion to test the system, and additional monitors that observe the system to compare the current parameter to a range of predetermined allowed values. The component selection step takes place in a typical project, but with the addi-

Figure 1. Typical design steps

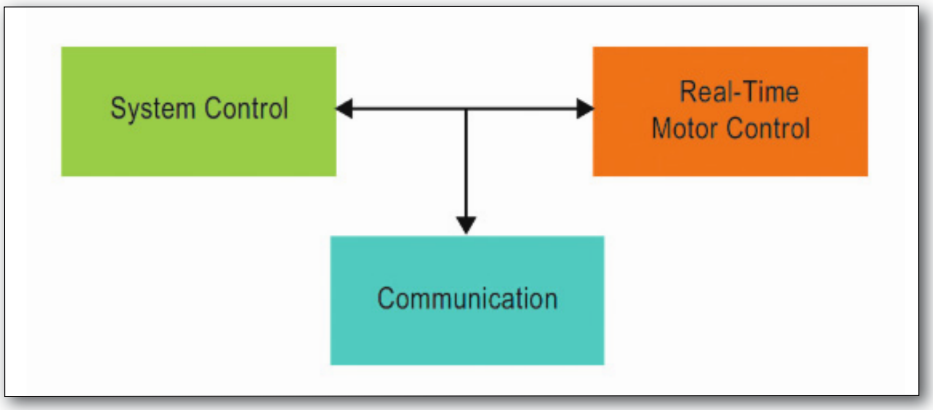


Figure 2. Architecture development

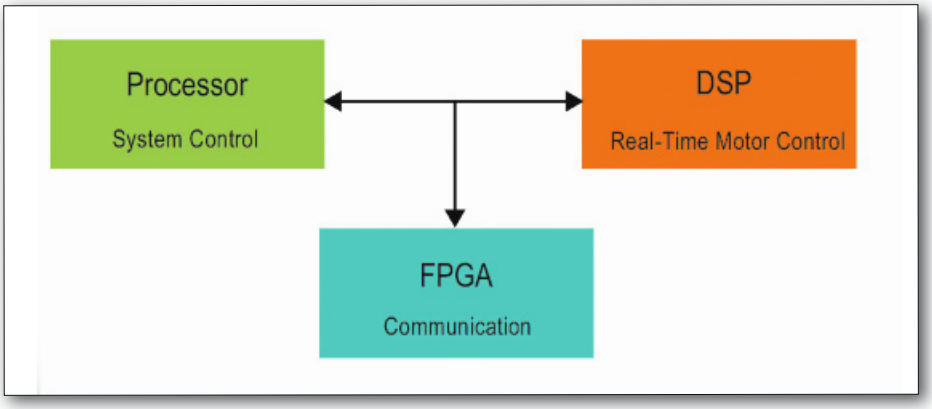


Figure 3. Component selection

tional need to ensure that the components and IP functions allocated and selected are suitable for use in a safe application. For the selection, it is important to consider the residual error probability, which is used as a basis to calculate the total failure probability (FIT) of a product and finally the achievable SIL. Partially, this can be achieved through gathering the required device and design tool data and information to ensure that products are used broadly by a wide range of users, in such a way that they are sufficiently free of systematic errors or proven in use (for IP, for example). It can also be achieved through access to reports that provide error rates and reliability information for semiconductor products like processors or FPGAs. However, it is often difficult to get access to reliability reports for components and semiconductor products that provide the necessary information, especially for related design tools and IP used for the application.

Complex system functions like communication protocols, memory interface IP used in the FPGA or processor IP embedded in the FPGA, such as the Altera Nios II embedded processor - typically used to run the software stack for industrial Ethernet protocols in drive applications - need to be analyzed, tested, and qualified for safety applications as well.

In addition to the implementation of the application, certain additional functionality must be added to the design. Basic parameter monitoring functions, such as clock and power, and complex functions, such as data monitors that ensure correct system operations by observing the output from a pulse-width modulation (PWM), are required. It is required to implement functions that automatically identify failures, and transition the system into a safe state. Basic functions include ensuring that memory content has not changed due to external impact on the design, or monitoring system clocks to ensure they are driving the design within the specified system parameters (or failed due to failure of external components), and that power supplies are operational.

After development of the individual components, they are integrated to a safe drive implementation and tested for delivering the expected system functionality as well as providing the safety functionality that has been specified. The safety validation must ensure that the desired safety features are in effect and remain in effect during operation, for example to ensure that an external impact on the design has no negative effect on the safety function such as accidentally disabling it without being noticed by the system. Throughout the entire process, close cooperation with the assessor is required to ensure that the measures taken during the development process are reasonable

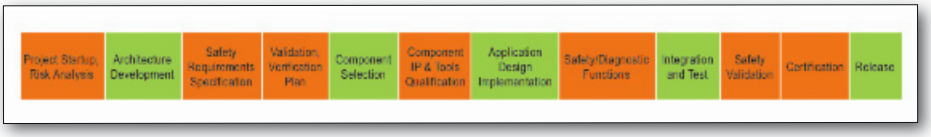


Figure 4. Design with safety steps

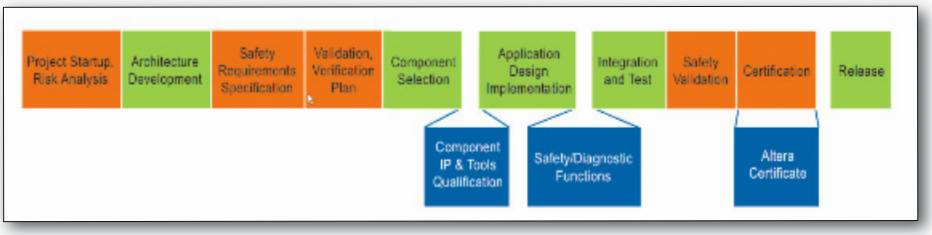


Figure 5. Design with prequalified safety steps

and provide the right level of safe functionality. Finally, the assessor certifies the product for functional safety and it can be released into the market. There are certain steps where semiconductor vendors like Altera can help with the process and reduce the effort for the development of safe applications. For example, having immediate access to semiconductor data, IP, development flows, and design tools that are already qualified for functional safety can provide a significant acceleration of the overall product development process.

Altera invested almost two years to achieve qualification for their products. The required test and usage data for IP and design tools and device reliability data are summarized and formatted in such a way that they can be presented for certification for functional safety. A TÜV-approved design methodology (V-Flow) was developed to address the specific needs of FPGA designs. Essential diagnostic functions were designed as FPGA IP and are provided as part of the functional safety package. This example of a drive with a safe I/O uses qualified FPGA design tools, Quartus II software version 9.0 SP2, from Altera and a suggested design methodology for the implementation of the application. In addition, a dual-FPGA implementation for the application, was used instead of external processors and DSP. The application is partitioned onto several Nios II soft processor cores. The first Nios II soft processor provides support for the communication stacks, the second handles the control of the system and the third Nios II processor is integrated into the motor control block. The motor control algorithm is partitioned so that its software portion runs on a Nios II processor and is accelerated by hardware blocks specifically developed for this applicator to accelerate the motor control loop. An external safety controller provides the redundancy required for a SIL3 application. This solution enables combining the safe controller with the field bus controller in a single FPGA, and uses the Altera SOPC Builder system integration tool to integrate the Nios II soft processors with the other IP blocks for communication, the encoder interfaces, and memory interfaces.

For low-level monitoring of critical but common diagnostic tasks in the FPGA, this example uses safety-qualified diagnostic IP blocks provided by Altera. These diagnostic IPs, designed to the IEC 61508 specification, perform common diagnostic functions such as the following. 1) Cyclic redundancy check (CRC) calculation - this calculation is useful in many systems and is particularly useful for fieldbus applications. 2) Derived clock checking - this core looks at the presence and frequency of clocks in the system. 3) SEU check controller - this block works with the built-in soft error checking hardware in the device to monitor changes brought about by so-called soft errors. Since the implementation of these hardware IP cores is in the FPGA logic area, the system processor is relieved of these tasks.

The design implementation follows the provided recommendations. In the area of qualified methods, Altera took the IEC spec and analyzed the FPGA design methods and related clauses. From this analysis, a tool flow document was produced. The V-Flow and the documentation that comes along with it maps all steps in the design of a safe application for Altera FPGAs to the IEC specification and its requirements. In addition, it explains which tools are used for the specified design steps. Specific chapters in the IEC specification are discussed and an explanation is provided to guide the user to follow the right development steps for the development of a safe application.

Altera provides a TÜV-qualified Functional Safety Data Package that covers qualified development tools, qualified IP, and qualified silicon data for devices under a specific tool flow. The documentation and data that the assessor needs for certification are included and provided in a format that matches precisely the IEC 61508 specification format so they can easily be processed by the assessor. Having this documentation available in the right format saves a significant amount of work for the documentation of the safety project. In the reliability report included in the Functional Safety Data Package, an extensive analysis of the statistical information about the reliability of Altera FPGAs is provided. All the necessary information to calculate failure-in-time (FIT) rates is part of the provided documentation, including a guideline that explains how to perform this calculation so that it can easily be presented to the assessor for certification. ■

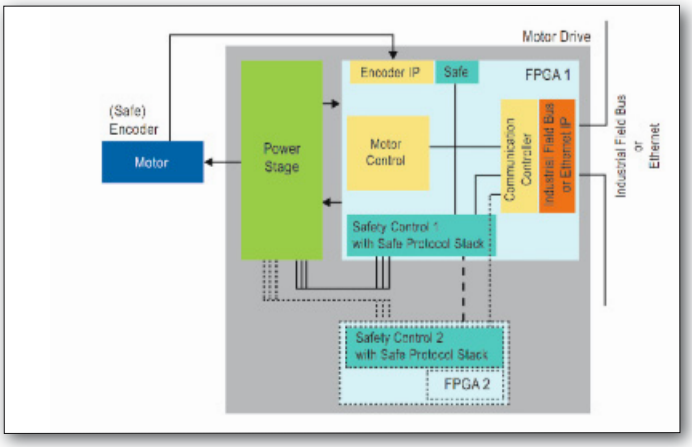


Figure 6. Dual-FPGA implementation of a safe drive

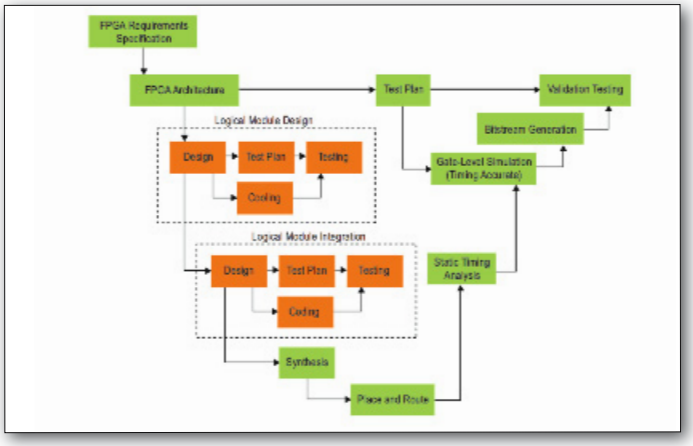


Figure 7. Tool flow for a safe design

Product News

TI introduces InstaSPIN-FOC motor control solution

Motor control system designers can now concentrate on differentiating designs rather than spending weeks and months tuning their motor control systems. With the new InstaSPIN-FOC solution from Texas Instruments, designers can now identify, tune and fully control (through variable speeds and loads) any type of three-phase, synchronous or asynchronous motor in five minutes or less.

News ID 16923

Toshiba: ARM Cortex development board for motor control

Toshiba Electronics Europe has announced a pre-configured development board for rapid implementation of motor control applications using its ARM Cortex-M3 family of microcontrollers. Developers can use the low-cost 'SigmaBoard' as a starter kit, as a reference design, or as a stand-alone solution for field-orientated control/vector control of brushless DC motors with ratings to 36V and 2A.

News ID 16972

Digi-Key opens European customer support center

Digi-Key is expanding its global footprint with new sales and customer support resources covering the EMEA region. The company today announced its regional sales leadership team and the opening of a new European sales and support office in Munich. Offering regional support to its EMEA customer base, Digi-Key appointed a team of experienced sales leaders, charged with supporting an existing roster of over 41,000 EMEA customers while expanding awareness of Digi-Key to both the design engineer and the higher volume Production Business buyer. Additional resources covering the Nordics, the Baltics, and Eastern and Southern Europe will be announced within the next 90 days.

News ID 17010

Telit expands Qualcomm portfolio with new LTE concept product

Telit Wireless Solutions announced the expansion of its long-standing relationship with Qualcomm Technologies. The complete portfolio allows Telit to offer form-factor compatible Qualcomm Technologies-based solutions for CDMA, UMTS and LTE radio technologies to address the communications needs of M2M and Internet of Everything application developers.

News ID 16888

TI: SoftwarePac features production ready PHY and transport software

Texas Instruments announced two new software packages for its KeyStone-based multicore System-on-Chips. The first software offering is a new production ready small cell Physical software package, enabling developers to quickly, easily and cost effectively design highly differentiated small cell base stations. The second software offering is a transport software package for wireless and other network-oriented applications.

News ID 16976

Microchip: BodyCom technology uses human body as low-power communication channel

Microchip announces its BodyCom technology, which provides designers with a framework for using the human body as a secure communication channel. Compared to existing wireless methods, BodyCom technology provides lower energy consumption, whilst further increasing security via bidirectional authentication. BodyCom technology is activated by capacitively coupling to the human body. The system then begins communicating bidirectionally between a centralised controller and one or more wireless units. There are many applications where secure wireless communication is essential, and there is no more secure channel than the human body.

News ID 16930

Toshiba: new line-up of image recognition processors for automotive

Toshiba Electronics Europe is offering an expanded line-up of Visconti image recognition processors with the launch of the Visconti3 series. The first device in this new series, the TMPV7528XBG, is enhanced by the integration of additional processor cores. Toshiba developed the Visconti series of image recognition processors to advance the creation of camera-based vision systems for automotive applications.

News ID 16959

More information about each news is available on www.Embedded-Control-Europe.com/ece_magazine
You just have to type in the "News ID". —

Savings all along the road with LEDs

By Wolfgang Reis, EBV

The fact that some LED components can be recycled is not just a positive aspect in environmental terms, it also results in lower disposal costs. There is much less of an LED left at the end of its useful life than of other types of lamp. LEDs offer many different savings: They do not have to be cleaned for example, nor – despite their 50,000 hour service lives – do they need maintaining. And maintenance can be very expensive in some cases, as the following example demonstrates. If a defective bulb causes a traffic light to fail, it is not merely a matter of the cost of a new light, but also of the time and effort for staff to come out and replace it; temporary traffic control by the police where appropriate; and possibly additional required materials. The economic loss resulting from traffic congestion is a further factor. Though the acquisition cost of an LED and the associated operating unit is higher than a conventional lamp, the savings over a period of years far outweigh the difference in initial outlay, because LEDs last in some cases 100 times longer than bulbs.

In order to deliver the light provided by conventional lamps, multiple LEDs are required. This does mean that the cost of lighting by LED is initially higher. It should be remembered, however, that the efficiency of LEDs is higher and so energy costs will be lower. A conventional 12 lm/W bulb uses three times more electricity than a white LED with a light output of 40 lm/W to attain the same level of brightness. Also, LEDs generate less heat, so the cost of air conditioning is reduced. The story is similar with regard to the use of LEDs in vehicles. The additional electronics required, the higher numbers of LEDs and their higher unit costs mean that the purchase price is higher. However, manufacturers are able to market LED-powered lights as a profitable optional extra, thereby also meeting the legal requirement to cut emissions. Moreover, vehicle

owners profit from reduced fuel consumption. The reason is that a generator driven by way of a belt by the engine generates the electrical energy needed for the vehicle. When more power is needed, the mechanical resistance of the engine increases, in turn increasing the fuel consumption. When LEDs are used, less electrical energy is needed. The resultant reduction in power consumption is important to the automotive industry not only because it helps cut CO2 emissions in line with legal requirements. Government moves to make driving with daytime running lights mandatory at all times are also leading motor manufacturers increasingly to fit LEDs.

According to the German Federal Highway Research Institute (Bundesanstalt für Straßenwesen), daytime running on conventional bulb headlights results in an additional consumption of 0.052 litres per 100 km, while the additional consumption with LEDs is 0.02 l/100 km. In , this would mean the annual additional fuel consumption resulting from permanent use of daytime running lights would be around 0.3 per cent of the total with bulbs and 0.1 per cent with LEDs. In other words: the total cost of cars driving permanently with their dipped beam headlights on (daytime running lights) resulting from the increase in fuel consumption in Germany would be 630 million euros. Over the long term, daytime running lights using LEDs would cut that cost to 60 million euros. Another factor is that LEDs are so long-lasting that they would even outlive the vehicles in which they were fitted.

Assuming that LEDs are operated within the limits specified by the manufacturers with regard to current and ambient temperature, and no environmental factors such as damp or chemicals lead to the premature destruction of the LED, the likelihood of a high-quality LED suffering a total failure over its lifetime is negligibly small. Failures of LED lamps usually result from defective or ageing soldered points; the LED itself remains operative. It should, however, be borne in mind that there is a difference in lifetime between the various colours, as they are made by different technologies. It can generally be assumed that LEDs in red, orange and yellow will age much less than green and blue – and thus also white – LEDs. In typical vehicle operation, red, yellow and orange LEDs attain service lifetimes of around 7,000 hours. Operating at normal ambient temperature at 80 per cent of the application-specific maximum permissible current, they attain around 10,000 hours, and at 50 per cent around 100,000 hours. If white LEDs are operated at half the starting current, their lifetimes can be expected to double. Double life can also be expected if the LED is operated at an ambient temperature 30 Kelvins below the starting value. In contrast to bulbs, LEDs are still lighting at the end of their lives, though at "time of death" their light intensity has fallen to 50 per cent of its original level.

Consequently, the decision as to which light should be used in applications in which replacement is complex and costly is easily made in favour of the LED.

Colour control of displays with high colour fidelity

By Frank Krumbein, MAZeT

This article describes the True Color sensors that are available as an IC or board solution developed by MAZeT.

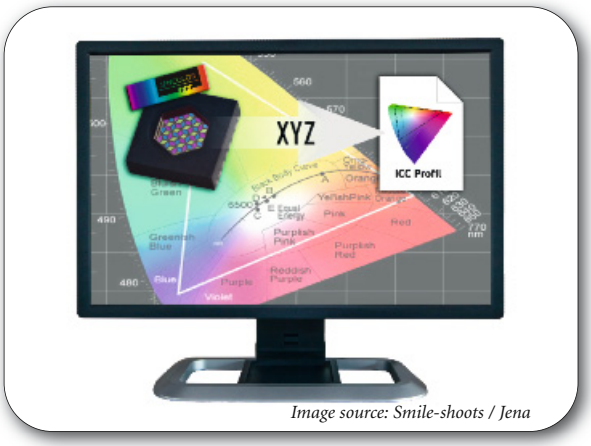


Image source: Smile-shoots / Jena

Displays, monitors and projectors are becoming more and more important in everyday life. From computer screens, tablet PCs, smart phones, and point-of-information devices to TVs and video walls for large-scale LED panels, the application range in the public, private and industrial sectors is steadily increasing. The user expects a high contrast ratio and brilliant colours. This results in a higher demand for so-called True Colours, driven by industry standards but also by a generally increasing number of users demanding higher-quality in colour applications. This characteristic, in conjunction with long-term stability over the entire lifetime and low energy consumption, is progressively becoming a distinctive selling point for high quality products. LED technology provides higher colour brilliance with increased service life compared to traditional display technologies.

However, being able to offer consistent True Colour technology via LED backlights in all conditions and over the entire lifespan requires certain precautions. Temperature, aging and technology-dependent errors and tolerance limits of the light source, optics, mechanics and electronics need to be corrected. This must be performed within the factories of the manufacturer at defined intervals and as a special service. This is especially true for LED-based light sources, where colour and brightness vary greatly due to temperature influences or aging of the system. Correction of the light sources during operation and integrated within the device requires independent and stable operating conditions of the optical sensor. True Colour sensors based on interference filters that are small, fast and cost-efficient, and that measure colour based on standards (for example: CIE1931 or DIN5033) without aging or temperature drift effects over the entire life time, are an ideal basis for color management and control options of light sources.

In medical engineering it is important that screens of diagnostic devices are capable of a high contrast ratio for detailed display options. Display colours based on an LED system show colours that shift depending on the operating time and heat management of the device. Sensors are used for monitor calibration in medical displays for fast and absolute measurements, to ensure accurate display of colours during operation, which are required by international medical standards. A correct diagnosis can only be made if accurate colours are displayed, whereas slight colour shifts could lead to a misinterpretation. Another option is to use external measurement devices to ensure suitable correction or calibration methods. To date display calibration has been performed by calibration laboratories at high costs and with great efforts. There are so-called colorimeters - external devices - that display users themselves can use for the calibration process. However, these devices require a certain amount of expertise and bear high initial costs. These devices vary depending on the technology used: spectral measurements tend to be expensive and require a high effort, while RGB sensors lack the required value accuracy. An ideal solution for the display market would be an auto-calibration method, which occurs invisibly in the background and provides a real-time benefit without additional user effort.

Video walls or screen network systems that consist of multiple displays have high demands regarding uniformity of colour and brightness. It is the goal to generate a unified picture impression, rather than a fraction of single images regardless of the operating and working conditions. The number of outdoor and semi-outdoor display systems for applications is constantly increasing. These systems are used as interactive terminals with multi-media properties to process information. All displays, light engines or projectors related to the video wall display should work with the same colours or colour temperatures so as not to distort the overall output. In contrast to this aspect, it is a challenging task to re-calibrate larger outdoor systems without high maintenance costs or special monitoring equipment, which is used externally on the screen. With these facts in

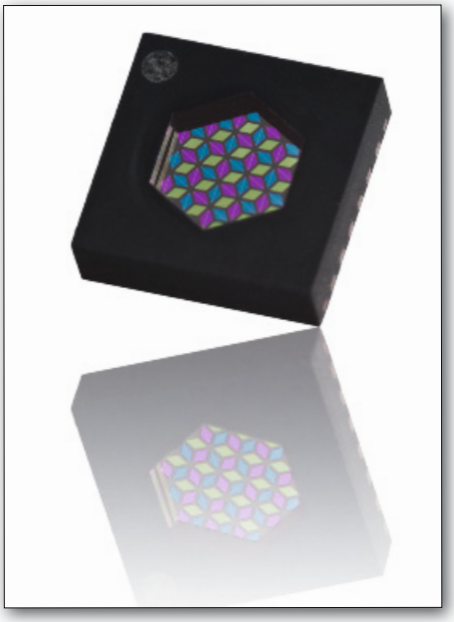


Figure 1. The True Color sensor MTCSiCF enables colour measurement based on the CIE1931/DIN5033 standard.

mind, alternative approaches are required that are either applied within the displays via backlight or light engine control, or allow remote monitoring of display segments. Similar approaches are found in alternative applications, for example the lighting industry, where mixed LED light sources that require to maintain specific colour temperature use feedback control-loop solutions.

The colour measurement of such applications is performed by compact JENCOLOR True Colour sensors. Supplemented with appropriate signal electronics, they enable new opportunities for device manufacturers and inline colour measurement of light sources and displays. The semiconductor-based sensors with XYZ interference filters are fast, cost-efficient and enable long-term stable colour detection and absolute colour measurement based on the CIE1931/DIN5033 standard. These sensors are capable of measuring colour differences within the colour space that are beyond the capability of the human eye. MAZeT offers these kinds of True Color Sensor ICs in various packages and embedded solution options including calibration libraries. (Sensor IC, evaluation boards for various applications).

The True Colour sensor IC MTCS is a miniaturized colour sensor for colour measurements based on the tristimulus procedure. The difference between usual colour sensors with absorption filters and RGB detection is that the MTCS can perform colour measurements with a spectral sensitivity based on the accuracy and performance of but better than the human eye. The standard values for the description of the colour areas X, Y and Z are a result of the emitted radiation and the spectral tristimulus function based on the colorimetric principle of True Color sensors. A nearly spectrally identical simulation of the CIE 1931 standard observer is required for a precise color measurement of emitted sources based on human eye perception. The quality of the viable colour measurement depends on the quality of these factors. Every variation of the standard observer values increases the total error of the colour measurement system. Depending on the task, the measurement system requires certain accuracy, as measurement error varies from the nominal value, even after a previously performed calibration. This deviation is defined as measurement error delta (for example ∅E for the deviation within the Lab-graph or ∅u'v' for the colour area error within the Lu'v'-graph) and is used for colour measurement applications. Certain factors like the measurement procedure, absolute and repeat accuracy of the sensor, lighting, calibration and disturbing sources of the system environment are the determinants of the requested accuracy levels.

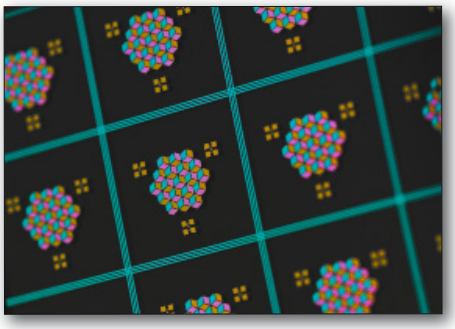


Figure 2. The JENCOLOR sensors consist of spectral filters that are based on human eye perception - that is standardized in colorimetric tasks based on CIE 1931.

Currently the MTCS colour sensors are the only miniaturized sensors based on the scaled tristimulus function. The sensor signals XYZ can directly be evaluated as colour areas within the colour graph. After calibration and under usual measurement conditions is possible to achieve values better than the perception limit of the human eye („Better than the human eye"; ∅E<3; ∅u'v'<0,002).Therefore True Colour sensors are suitable for any applications where the human eye is used as standard of accuracy comparison. The basic accuracy of the MTCS colour sensors uses a PIN diode technology with optimized spectral sensitivity for the visible range.

The resulting tristimulus sensitivity is a combination of the basic accuracy and specific filter options of the higher level layers. The three filters are explained by specific layer designs consisting of high and low level refractive layers and the combined interference effect for various wavelengths. These interference filter layers are directly patterned onto silicon wafers or glass carriers by a lithographic procedure, and therefore are temperature independent and long-term stable filters. To adjust the sensitivity to the standard values X, Y, and Z, sensor data is scaled to a known white via various combination colors. Additionally this can be corrected globally or locally via matrix methods and can be transformed to any colour space at a high accuracy.

Alongside the choice of the right JENCOLOR sensor for lighting application, the choice of electronics is essential as well to achieve a high bandwidth, dynamic range or the option of synchronous measurements of multiple devices. These tasks are performed by MAZeT sensor signal IC MCDC04, which is used as internal current-to-digital converter. The photo currents of these detectors are processed digitally on-chip using an integrated continuous-time system for load balancing, whereas the data out is processed via an I²C interface at 16-bit resolution. The full scale range is (FSR = 5pA to 20µA) adapted to the specific application or by adjustment and variation of the reference current (40nA to 40µA) as well as the integration time. The ADC is operated at a constant frequency and changes the resolution of the AD conversion via integration time. This leads to a resolution of 20 bits at maximum integration time (TINT = 1s) and 12 bits with minimal integration time (TINT = 1ms). The IC is temperature-compensated and features the possibility of external triggering of measurements. Due to the internal current-to-charge conversion in the related parameters, the signal-IC is combined with True Color sensors for applications requiring high light variance, for example in applications where light colours need to be measured at varying conditions.

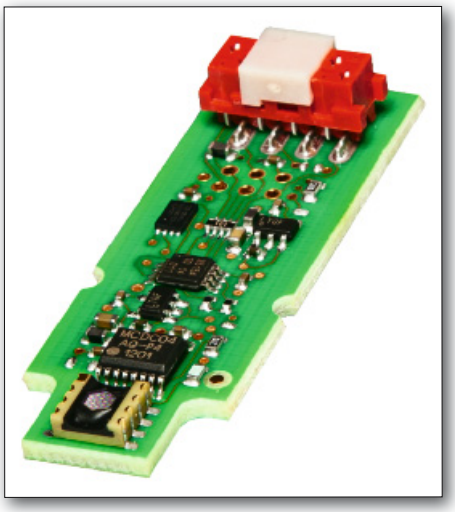


Figure 3. True Color solutions are available as ICs or board solutions optimized for the lighting industry.

The True Color sensors are available as an IC or board solution developed by MAZeT. They are commonly used in measurement devices or systems of various manufacturers, for example, within the calibration system Mii 2 mobile colour analyzer developed by Premosys enabling to manage the colour intensity and contrast of displays with pin-point accuracy.. The system is applicable to different display types, regardless of CCFL, LED or RGB backlight, for both narrow- or wide-range. The device provides excellent repeatability, is easy to use and allows a very fast calibration of displays.

The achievable accuracy lies in a region that was previously only manageable by very expensive measurement systems. The system is available in different versions with USB or RS232 interfaces. It is possible to perform up to eight base calibrations in addition to thirty individual user calibrations to meet the demands of customer-specific displays. Likewise, flicker measurements can be performed. The integrated temperature sensor compensates the temperature shift during the measurement. The integrated design ensures the long-term stability of the measurement values. The measurement device is calibrated individually, and can always be recertified, so that the system can be used as reliable test equipment for several years.

Similar solutions for screen measurements exist from other companies. The Brontes Colorimeter from Admesy was developed for display applications where colour rendering is extremely important and long-term stability must be guaranteed without re-calibration. In addition to the high accuracy, an extremely high measuring speed is a selling point. ■

Product News

■ Atlantik presents Greenvity s HomePlug Green PHY for LED lighting

Atlantik Elektronik introduces the latest member of Greenvity Hybrii family, the new Hybrii-Mini GV7013. This chip is compatible to the PLC HomePlug Green PHY for Smart Grid applications and is ideal for intelligent LED lighting systems over long distances within the commercial, public and private sector. The GV7013 enables a robust and reliable two-way communication of remote-controlled street lights up to digital signage applications. In residential and commercial buildings the Hybrii-Mini PLC also enables larger transmission distances through multiple walls and ceilings.

News ID 16878

■ ams: intelligent LED driver for mobile phone cameras

ams introduced a new intelligent LED driver for mobile phone cameras that maximizes the brightness of the flash without causing the phone's battery to fall below its minimum operating voltage. The AS3649 LED driver uses an innovative "diagnostic pulse" – a burst of controlled high current lasting a few milliseconds – immediately before every flash operation. During this pulse the device measures the momentary voltage across the terminals of the phone's battery. On the basis of this measurement, it reports a value for the highest flash drive current the battery can sustain, up to a maximum of 2.5A, without dropping below its minimum voltage and triggering the phone to reset itself during the main flash.

News ID 16965

■ Electronic Assembly: 5.7" color display includes touchscreen capability

The EA eDIPTFT57-A intelligent display from Electronic Assembly is, for a variety of reasons, the ideal candidate for implementing an interactive control in mechanical engineering or industrial electronics applications. The high-contrast screen, for example, which measures 5.7" in the diagonal and has LED background illumination, offers a crisp, colorful resolution of 640 x 480 pixels.

News ID 16979

■ FTDI: easy-to-use graphic controller for wide-ranging display applications

Addressing the need for ever more advanced forms of human-machine interaction, FTDI has announced the release of the FT800, the initial offering in its Embedded Video Engine (EVE) family. Targeted at cost-effective, intelligent QVGA and WQVGA TFT display panels, the FT800's object oriented approach renders images in a line by line fashion with 1/16th of a pixel resolution, eliminating the expense of traditional frame buffer memory. Supporting 4-wire resistive touch sensing with built-in intelligent touch detection and an embedded audio processor allowing midi-like sounds combined with pulse code modulation for audio playback, the controller's functionality sets new industry benchmarks.

News ID 16915

■ ARM: adoption of ARM big.LITTLE technology accelerated

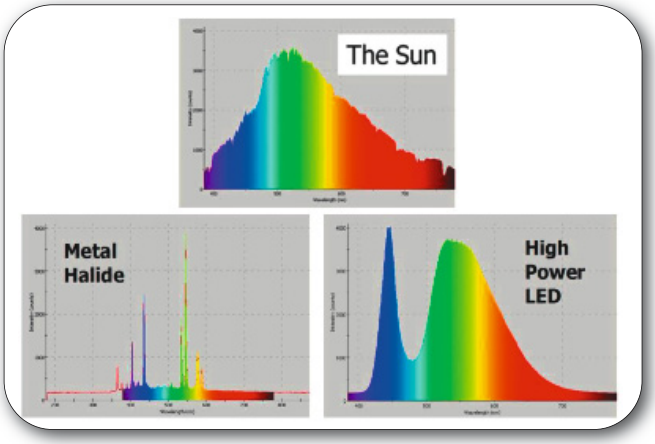
ARM unveiled that its big.LITTLE processing technology has been adopted by many of the world's leading mobile chip manufacturers. Samsung and Renesas Mobile have already announced their plans, and subsequent implementations will be revealed during 2013 by five more companies including CSR, Fujitsu Semiconductor and MediaTek. ARM big.LITTLE technology saves up to 70 percent of processor energy consumption in common mobile workload tasks, essential as the performance of the smartphone has jumped by 60x since 2000 and 12x since 2008, causing a massive increase in both content generation and consumption.

News ID 16931

Lighting industry continues to move towards the adoption of LEDs

By Stephan Greiner, Cree

This article reviews the many benefits of LED technology which support its increasing acceptance throughout the lighting industry.



Spectral concentration of various light sources

A technology that was once known for tree lighting during the holidays and headlights on the newest cars is now making its way into the commercial and residential sectors – from schools and office buildings to gas stations, hotels and homes. More and more facility managers and electrical contractors are making the switch to LED lighting to save big on energy and maintenance costs. Although monetary payback savings and longevity often drive the shift to LED lighting, there are several other benefits. Below are a few reasons why LED lighting is quickly rising to the top as the preferred lighting option.

Illuminating a space depends largely on the desired outcome. For example, warehouse lighting tends to be brighter than residential lighting because workers need the additional illumination to perform their tasks. Contrary to the common belief that LED lighting emits a harsh white light, the technology has now become so advanced that it can achieve a wide range of colour temperatures (from cool to warmer whites) to address more applications than ever before. As the human eye adapts to various light settings, it is important to have variation; brighter lighting in an office environment and warmer (yellower) lighting in the evening. Cree LED lighting products fall between 2700K and 4000K colour temperatures. In order to achieve optimum illumination for a given application, luminaire design starts with the LED components within the fixture, not the physical aesthetics of the fixture. The colour temperature of the lighting fixture is often determined by the LED components which serve as the light source. Luminaire designers select the LED components for the fixture based on the desired end lighting effect. By going LED, lighting specifiers can attain the most appropriate lighting colour for their applications while benefiting from the energy and maintenance savings associated with using this technology. The same varied colour temperatures and energy efficiency are not available with incumbent light sources. For example, metal halide fixtures used for exterior parking lot lighting end up consuming high amounts of wattage. This isn't the case with LED luminaires.

Not only does LED lighting provide a wider range of colour temperatures than previous options, but it also has a greater colour spectrum to more closely replicate natural daytime lighting. In other words, objects under LED lighting look the most similar to what they would look like under the sun. The colour rendition can be measured using the Colour Rendering Index (CRI) where 100 is the highest marker and represents daylight. A CRI in the 80s range is generally good enough for most applications while a CRI of 90 (where high-quality LED luminaires range) is nearly identical to natural daylight. This is achieved because LED lighting has greater intensity at the various wavelengths than metal halides.

Additionally, the high colour quality of LEDs remains consistent longer than current options. LED lighting has a low light depreciation rate so illuminated areas have uniform lighting that lasts longer than technologies like high pressure sodium or metal halides. Older lighting technologies diminish in colour quicker, resulting in different coloured lighting fixtures throughout the illuminated space. Due to the stable nature of LEDs (a solid state lighting technology), areas illuminated by LED luminaires will be continuously lit without interruptions, unlike fluorescent fixtures that flicker.

Due to the nature of LED technology, there are many control possibilities, such as dimming. The LED source can be operated through a wide range of power and output, enabling many applications with adaptive illumination to right-size the illumination while maximizing energy savings. With dimming capabilities, it is possible to adjust illumination based on the changing requirements of the application. This can be accomplished with systems ranging from network-based closed loop dynamic monitoring and control, to something as simple as a manual dimming control system. In general, it is easier to justify greater light control with

an LED-based system because LED fixtures are often sold with dimming as a standard feature. Therefore, daylight harvesting and dimming capabilities are most cost-effective with LEDs. Embedded control protocols enhance dimming capabilities, demonstrating the ability for LEDs and controls to work together seamlessly.

Cree, for example, just entered into a first-of-its-kind agreement with Lutron Electronics Co., Inc. to embed Lutron EcoSystem technology on a chip into its luminaires. By using energy management solutions such as Lutron EcoSystem technology, LED lighting can significantly reduce building owners' operating costs and continue to deliver faster payback. Digital control and dimming of LED fixtures can significantly extend LED lifetime while also allowing flexibility to reconfigure and improve occupant experience in any space.

Optical control is also crucial to proper illumination. Continued engineering advancements in LED technology can improve optical efficiency, maximizing illumination to desired areas with less light spill-off. For example, Cree NanoOptic Precision Delivery Grid optic technology featured in the XSP Series LED Street Light efficiently delivers light to the street, making communities appear cleaner and safer.

LED lighting offers several secondary benefits. LEDs are mercury-free, UV-free and low heat emitting. These features increase the environmental friendliness of a building, while protecting products and supplying visitors with a comfortable atmosphere. LEDs offer the perfect alternative to other high-efficiency light sources, like compact fluorescents and high intensity discharge fixtures, which contain toxic mercury vapour. Problems occur when these lights break and mercury escapes as a vapour that can be inhaled and as a powder that can seep into textiles. These lights must be properly disposed of in order to prevent mercury from poisoning landfills. Additionally, since the mercury vapours need to warm up to actually emit light, these fixtures do not turn on instantly and occasionally flicker. LED luminaires, however, are instantly on, do not flicker and do not contain mercury.

Another benefit of LEDs is that they are UV-free. Ultraviolet rays can cause degradation to artwork, apparel, furnishings and even food. This lighting quality is particularly important in grocery stores. Given their relative size and wide variety of consumer areas, grocery stores must pay attention to both efficiency and light quality. LED lamps deliver bright, UV-free light to attract consumers to goods while helping keep produce and other foods fresher for longer. For example, UV rays cause the colour of fresh meat to fade and accelerate the development of rancidity in the meat fat.

Along with being mercury-free and UV-free, LEDs also emit a lower amount of heat compared to other light sources. Most of the energy emitted from incandescent bulbs is converted to heat instead of light. Touching an incandescent bulb that has been turned on for a while can even cause a harmful burn. Since LEDs consume significantly less energy, they do not emit as much heat. This is especially important to consider in terms of warmer weather environments and cooling costs.

Many LED bulb fixtures are also equipped with a thermal management system that uses an integral heat sink to conduct heat away from the individual LEDs and transfer it to the surrounding environment for optimal performance. The advanced heat sink and heat piping technologies are integrated to maximize the cooling effectiveness of each LED lamp. Moreover, LEDs are not as sensitive to changing weather patterns, like cold weather that can be detrimental to fluorescent lighting. Unlike metal halide fixtures that need to cool down before being turned on again, LED lighting does not have this heat issue and turns on instantly. Additionally, since LED is a solid state technology, LED luminaires tend to be more durable. Components do not break as easily as other lighting options, specifically metal halides. A prime application example of this is a parking garage with multiple levels. These levels are not as rigid as the ground floor, so as cars drive by the structure will vibrate causing disruptions in the lighting quality of metal halides and high-pressure sodium light fixtures.

The benefits listed here are some of the main reasons why LED lighting is growing in acceptance and use in many industries around the world. Aside from the much expanded capabilities of LED lighting, which can be further maximized in the design process, LEDs are being designed with the intent to meet the undeniable requirements of the future. For example, the demand for adaptive lighting is expected to continue to accelerate as energy codes continue to evolve and become even more stringent to reflect advancements in the lighting industry. Unlike incumbent technologies of the past, LED technology is well-suited for such applications and is expected be at the forefront of this movement. Integrating LED solutions with adaptive controls allows for overall improvements in total cost of ownership through a combination of even greater energy savings and improved long-term luminaire performance and reliability. Through these and other innovations, LED luminaires are continuing to carve out a clearly defined and widely recognized place for themselves within the lighting market. ■

Product News

■ Cypress: touch controllers silence noise from even worst chargers and displays

Cypress Semiconductor introduced its next-generation Gen5 TrueTouch controller product line that delivers most noise-immune touchscreen control technology, shattering current standards for performance in noise from all sources. Gen5 offers unprecedented 40 volt peak-to-peak charger noise immunity measured from 1 to 500 kHz with an ultra-thin 0.5-mm cover lens and a finger-size up to 22 mm—the most stringent specifications used to measure any touchscreen controller. No competing controllers deliver noise immunity over 15 Vpp under these conditions.

News ID 16899

■ nanotron: industrial safety platform with swarm features

nanotron has launched a new product to revolutionize industrial safety applications: the swarm platform. The nanotron swarm platform consists of swarm radios controlled by a swarm application programming interface as well as swarm toolkits. It consists of swarm radios controlled by a swarm application programming interface as well as swarm toolkits enabling fast development and implementation of location-aware applications. Swarm is currently used for collision avoidance, secure access and virtual safety zones.

News ID 16951

■ EB achieves ASIL D and SIL 3 certification for tresos Safety OS

Elektrobit achieved its Functional Safety certification by the assessment agency exida Certification SA for the EB tresos Safety OS. Exida confirmed that the software is capable for use in Automotive Safety Integrity Level D applications such as electrical power steering. Additionally, the OS is certified for Safety Integrity Level 3 used in non-automotive projects. ASIL D and SIL 3 rank among the highest security levels for functional safety according to the ISO26262 / IEC 61508 specifications for electric and electronic components.

News ID 16941

Development process runs smoothly thanks to Eclipse

By Heiko Riessland, PLS Programmierbare Logik & Systeme

Are you one of the software developers that have to constantly deal with different target architectures, perhaps sometimes even within a single embedded project? Standardized development, test and debug tools can be very useful here, particularly when they are modular and extendable like the Eclipse framework.

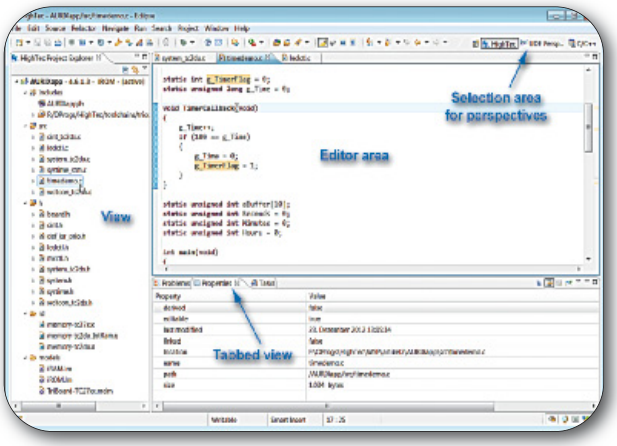


Figure 1. Structural concept of Eclipse simplifies the work of developers.

A favourite editor or preferred development environment provides plenty of opportunity for discussion by software developers of microcontroller applications. Surprisingly, there is obviously still a certain level of personal freedom in regard to this point; even in some large organizations with otherwise clearly defined processes. However, as a rule, in large companies the trend towards standardized tools is evident. Uniform tools and known operating concepts, of course, significantly reduce the expenditure needed to learn new target architecture and developers can concentrate on their main task. In order to ensure the necessary longevity and vendor independency, an open-source project - such as the Eclipse platform - offers ideal conditions for an efficient implementation of such intentions.

Eclipse was originally created by IBM for the Java programming language. Today, the Eclipse Foundation, a member-supported corporation based in Canada, is responsible for the further development. IBM still contributes with many of its own developers and also uses Eclipse technology in its own products. Since Version 3.0, Eclipse, which was originally developed as an integrated development environment (IDE), simply provides a framework. The Eclipse platform uses so-called plug-ins in order to provide the actual functionality. This highly flexible concept paves the way for very broad use as a universally applicable development platform. Both Eclipse itself and the plug-ins are implemented in Java. However, this does not mean that plug-ins cannot execute functionality from native code components. Eclipse graphical interface, which is based on the Standard Widget Toolkit (SWT), also sits on top of native GUI components of the respective operating system on which the Java environment runs. As with some plug-ins, Eclipse itself is thus not completely platform-independent; however, it is nonetheless currently available for 14 different operating system platforms.

The structural concept of Eclipse simplifies the work of developers. For example, so-called editors are available to them for building applications by writing source code, drawing diagrams, etc. Entry in the text windows takes place by conventional programming with support of the respective programming language via syntax highlighting and features such as auto-completion. Furthermore, graphical editors - for example, for Unified Modelling Language (UML) or editors with tree presentation for eXtensible Markup Language (XML) - are also popular.

Editors typically occupy a large part of the user interface, whereby several source codes or diagrams can be open in parallel. A tab view with so-called tabs at the top edge enables fast access. The actual editor window is surrounded by a further type of window, the so-called views, in which additional information is displayed. Examples of this include a project tree with all associated files, an Explorer view for displaying classes, functions, variables and type hierarchies as well as windows, which display the result of a build run or search results and enable a direct navigation to the respective source code position.

Fundamental components of the Eclipse concept include the so-named perspectives. These are complete preconfigured collections of menus, toolbars, editors and views. Despite the pre-configuration, the perspectives are adaptable to a great extent to the user requirements. User defined settings can be stored and loaded again later.

The Eclipse workspace is a further basic function, although not necessarily visible on the surface. When an installed Eclipse platform is first started, the user is asked to choose a workspace directory. From now on, all projects that have been created or imported are stored and organized in this directory. The advantage is that relationships between the projects now only exist of relative path information relating to the workspace directory. Hence, these are very easy to move. The individual developers of large project groups work with their local

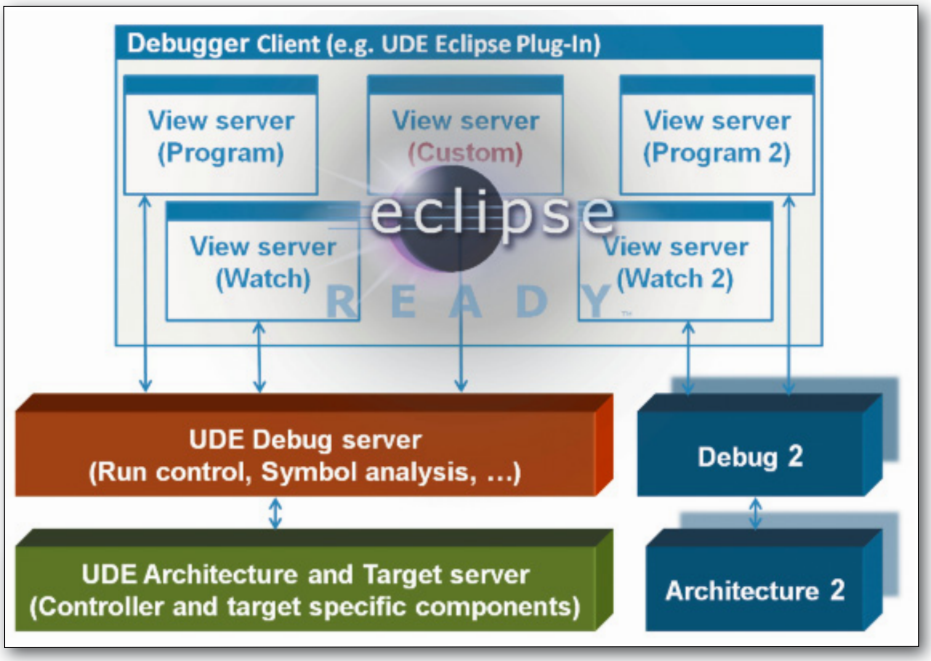


Figure 2. The component-oriented construction of the UDE with strict separation of function and user interface enables the implementation of a complete debug perspective within Eclipse.

workspace directories, whose specific location in the local file system is completely meaningless for the group. Therefore, with the workspace concept, Eclipse creates its own storage system in the selected directory based on the underlying file system. The otherwise usual rigid central file storage is not necessary here and is replaced by the repository of a version control system. External references are also no longer needed. All relevant information is imported or copied to the workspace directory.

Furthermore, with the C/C++ Development Tools (CDT), Eclipse offers a well-filled toolbox, consisting of several plug-ins of the Eclipse Foundation, for C/C++ development. It also includes project and build management, a powerful editor with syntax highlighting, navigation support and refactoring capabilities, as well as numerous functions based on static source text analysis such as the presentation of type hierarchy, call graphs, browsers for include files and macro definitions. What is more, a source code debugging extended with windows for memory, register and disassembler is provided. The implementation is based exemplarily on the GNU compiler and the GNU debugger (gdb).

0The debugger component of the Eclipse CDT is the only weak point for use as a cross-development platform. Its model is based on observation of the target in a suspended state, which is an approach that obviously does not cover the requirements of modern cross-debugger solutions. Unfortunately, the debugger component of Eclipse still does not offer any possibility to access the memory while the target is running and to update values in the debugger. Trace data for code coverage and code profiling, both must also be read and visualized without stopping the target, cannot be evaluated, and the presentation of peripheral registers, mostly several hundred with modern microcontrollers, is not possible.

This also explains why Eclipse support by emulator and debugger manufacturers has up till now mostly been limited to so-named call plug-ins. With their help, manufacturer-specific debugger user interfaces can be started from Eclipse and setting of breakpoints in both user interfaces or, for example, also the reciprocal opening of files even enables some synchronization. However, full performance for test, debugging and system optimization is only available in a separate tool of the debugger manufacturer. Another approach to upgrade the integrated Eclipse debugger is the retrofit of certain views for the special function registers (SFR) and real-time variables displays. However, the functionality here also ultimately mostly remains an unsatisfactory compromise between the debugger integrated in CDT and the manufacturer-specific user interface.

Thus, the only solution offered to this dilemma is the implementation of a complete debug perspective within Eclipse. The following example provides developers with the complete functionality of the Universal Debug Engine (UDE) from PLS, without having to make any compromises. This is made possible by the component-oriented construction of the UDE

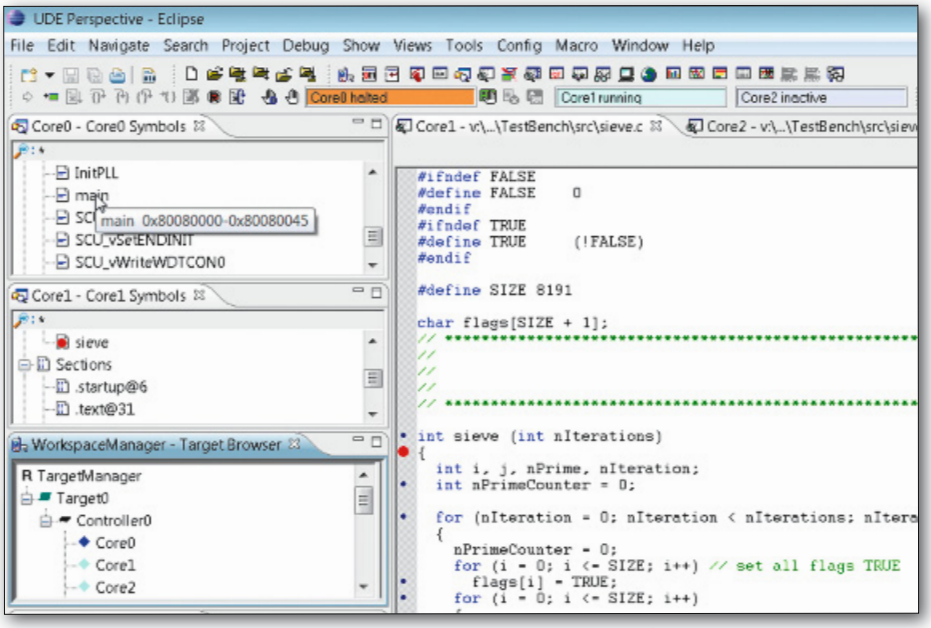


Figure 3. The UDE Eclipse plug-in even supports the management of several debugger instances for multicore debugging without limitations.

with strict separation of function and user interface. The UDE Eclipse plug-in, a relatively thin wrapper written in Java, provides the connection between Eclipse and the functional components of the UDE. For this purpose, besides the SWT-based window and menu services of the Eclipse workbench, the debug interface of an installed CDT as well as interfaces of the SWT to Win32 native functions are also used. Hence, the UDE Eclipse plug-in - as also the Universal Debug Engine (UDE) - is only available on Windows platforms. The installation takes place with standard mechanisms provided by the framework. Eclipse views are used for display of the debugger-specific windows and furthermore, synchronization with the open C/C++ editors is carried out.

Display of all UDE windows in Eclipse views enables the unlimited use of cross-debugger features, which far exceed the standard CDT debugger. These include, for example, configurable periodic refresh of all target memory displaying windows also during runtime of the application, graphical display of application variables, profiling and coverage functions, RTOS support, display of peripheral registers (SFR) in clear text as well as trace data analysis. Even the management of several debugger instances for multicore debugging is supported without limitations. A debug session can be simply defined as launch configuration and started from the C/C++ editor in own cross-debugger perspective. Breakpoints can be set both in the C/C++ editor and in the debugger itself. Their display takes place, the same as those of the instruction counter, synchronously in all perspectives. Furthermore, the use of C/C++ editors in the UDE perspective is also possible. The paths of source files are read by the UDE plug-in direct from the workspace. This ensures an Eclipse typical consistency during the development phase.

This approach to a solution of a complete cross-debugger perspective as described combines for the first time the advantages of the universal, flexible Eclipse concept with the performance of a modern cross-debugger needed by the user and thus to some extent certainly sets the trend. The Eclipse plug-in is available for all Universal Debug Engine supported microcontroller architectures and families including TriCore, PowerArchitecture, Cortex, ARM and XC2000/XE166. In addition to adapted Eclipse platforms Ganymede (Eclipse 3.4), Galileo (Eclipse 3.5), Helios (Eclipse 3.6) and Indigo (Eclipse 3.7) from various compiler manufacturers, self-configured Eclipse CDT platforms of these versions are also supported. Support for Juno (Eclipse 4.2) with a completely new structured programming interface for plug-ins is in preparation for 2013. ■

Product News

■ Softing standardizes on IAR Systems' embedded development tools

Softing Industrial Automation continues to rely on embedded development tools from IAR Systems. The recently signed enterprise agreement allows Softing's development teams to flexibly shift licenses between their sites in Germany and Romania. They also gain high flexibility when it comes to the choice of platform, as the comprehensive IAR Embedded Workbench supports more than 7,800 MCUs within different architectures.

News ID 16920

■ Wind River joins OSADL to advance Linux in Embedded and Industrial designs

WindRiver has joined the Open Source Automation Development Lab). With its membership, Wind River will collaborate with other OSADL members to further promote and support Linux solutions for the embedded and industrial markets. Founded in 2005, OSADL fosters the development of open source projects in the areas of embedded systems and industrial design, including projects focused on real-time and safety-related systems, and special drivers for the Linux kernel required by the automation industry.

News ID 16916

■ IAR supports XMC1000 ARM Cortex-M0 MCUs from Infineon

IAR Systems announces comprehensive support for the XMC1000 family of 32-bit microcontrollers recently announced by Infineon. The support is available using IAR Embedded Workbench for ARM, which is a complete set of high-performance tools for embedded development. The XMC1000 family is based on the ARM Cortex-M0 core and features advanced peripheral functions. It is designed for use in low-end, cost-critical industrial applications, such as sensor and actuator applications, LED lighting, digital power conversion and simple motor drives used in for example household appliances, pumps, fans and e-bikes.

News ID 16874

■ LDRA: MISRA C:2012 compliance tools

LDRA announced the immediate availability of compliance tools for the recently announced MISRA C:2012 guidelines for safety-critical software. LDRA offers the most comprehensive and automated approach to meeting the MISRA C rules, with products that include a standalone rule checker as well as a portfolio of tools that integrates MISRA C compliance into the software development lifecycle. With LDRA's updated products that incorporate the latest MISRA C rules, developers can be assured that they are following the most stringent coding quality standards to mitigate liability and risk in software applications on which human lives depend.

News ID 16903

Creating a flexible solution for testing 802.11ad devices

By Spiro Moskov, Agilent Technologies

This article outlines some of the key problems in testing and presents a system configuration that enables detailed testing and analysis of 802.11 ad devices.

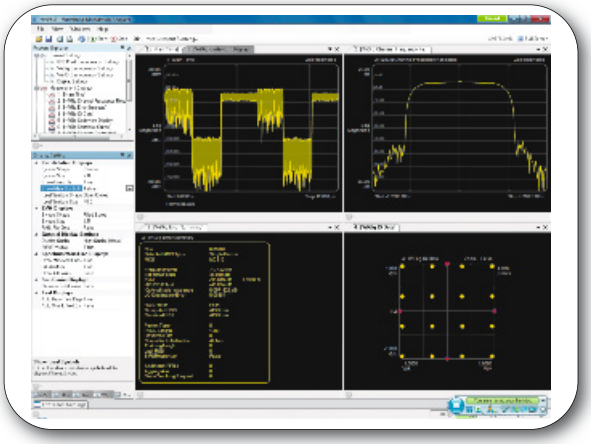


Figure 1. This example of EVM measurement was created using a test system configuration similar to the one shown in figure 2.

The IEEE 802.11ad standard is an up-and-coming technology expected to enable wireless connectivity of up to 7 Gbit/s in data, display and audio applications. Per the January 2011 draft standard, signals will occupy the unlicensed 60 GHz frequency band, and compliant devices will provide backward compatibility with the 802.11 standard. As a result, tri-band devices will operate at 2.4, 5.0 and 60 GHz. Many companies have launched product development projects and developers face challenges that stretch from system-level design to verification testing.

For example, thorough testing of 802.11ad transmitters and receivers requires three essential elements: arbitrary waveform creation; frequency conversion; and signal, modulation and spectrum analysis. In the development of new 802.11ad products, testing must address the transmitter and receiver portions of each device. In a tri-band device, signals have three key attributes: they operate at 2.4, 5.0 and 60 GHz; carry various modulation schemes; and have bandwidths in either the 20 MHz range (802.11a/g/n and 802.11b/g), 40 MHz range (802.11n), up to 80/160 MHz contiguous or noncontiguous (802.11ac), or 2.0 GHz (802.11ad). At various points within the radio block diagram the signals may operate in the baseband, intermediate frequency (IF) or radio frequency (RF) range.

As a general problem statement, the IEEE 802.11ad draft standard includes specific measurements with expected values for transmitters and receivers. Examples include receiver minimum sensitivity and transmit error vector magnitude (EVM; see figure 1). Going beyond the draft specifications, design teams may also want to verify the overall performance of a new 802.11ad device. In such cases, they will want to look at important measurements such as match, gain or loss through frequency converters, and nonlinear tests such as p1dB under various operating conditions. Thorough testing of 802.11ad transmitters and receivers at baseband, IF and RF requires three essential elements: arbitrary waveform creation; frequency conversion; and signal, modulation and spectrum analysis. The flexible and configurable test setup shown in figure 2 covers all these requirements.

Starting at the top of figure 2, waveform creation at baseband frequencies is accomplished with specialized software and an arbitrary waveform generator (AWG). In this case a 4.2 GS/s AWG is used to create highly accurate simulations of standard-compliant signals that can be applied to transmitters and receivers. Key features of the AWG include 12-bit resolution, up to 64 MS memory and advanced sequencing capabilities. The AWG is available with one or two output channels, and two units can be linked to provide four synchronized outputs. Each output channel has up to 1 GHz modulation bandwidth and up to 2 GHz I/Q modulation at carrier frequencies of up to 1.5 GHz. Characterization of device performance versus the standard also requires generation of impaired or corrected signals that mimic real-world issues such as fading, distortion, I/Q skew and carrier-to-noise problems. One way to accomplish this is with waveform-creation software that can download waveforms into AWG memory. Examples include SystemVue and Signal Studio from Agilent as well as MATLAB from The MathWorks.

Moving down the figure, IF-band frequency conversion is accomplished with an upconverter. This configuration uses a vector signal generator with optional wideband external I/Q inputs. As shown, the AWG is used to directly drive the internal I/Q modulator with I/Q modulation bandwidth of up to 2 GHz. A custom-designed upconverter provides frequency conversion to the RF range. A high-precision microwave analog signal generator provides a stable LO signal for the upconverter.

In the lower half of the figure, the custom-designed downconverter provides frequency translation to the IF band. In this configuration a high-performance oscilloscope (up to 32 GHz analog bandwidth) and an advanced signal

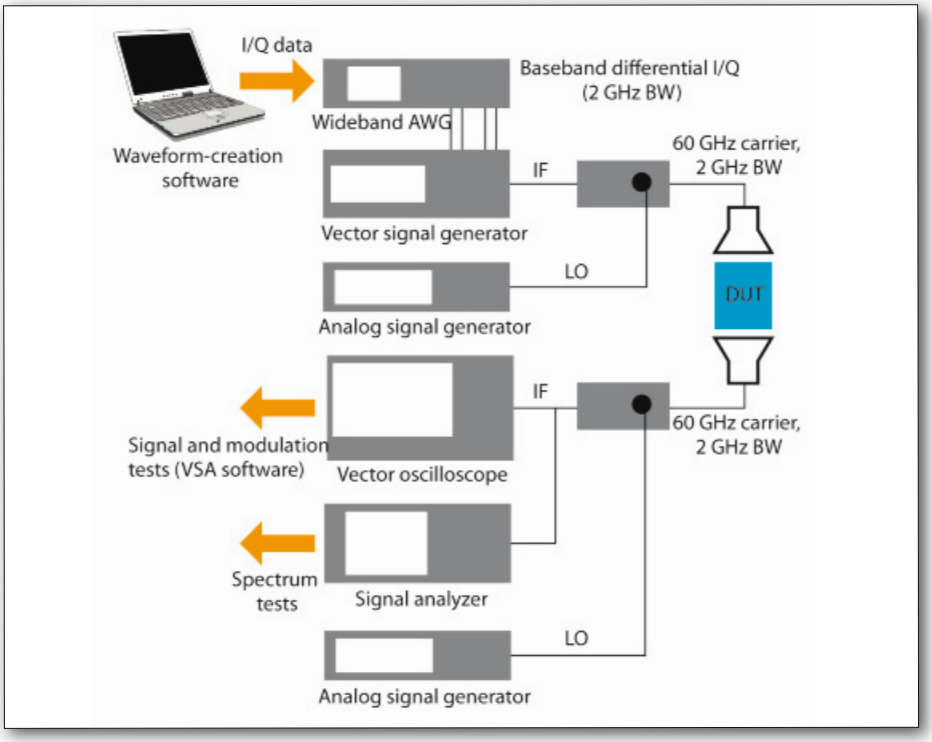


Figure 2. Thorough testing of 802.11ad transmitters and receivers requires a mix of capabilities: waveform creation, signal generation, frequency conversion, signal analysis, modulation analysis and spectrum analysis.

analyzer (with optional high-end frequency coverage from RF to millimeter wave) provide signal, modulation and spectrum analysis capabilities. This configuration also includes the Agilent 89600B vector signal analysis (VSA) software, which supports more than 30 hardware platforms and can run on a PC or inside newer Windows-based instruments from Agilent. The VSA software supports more than 70 signal formats, provides advanced demodulation capabilities, and performs measurements of EVM and other important signal characteristics. MATLAB is another important part of the receiver-side solution. Here, it provides a software environment for measurement automation and data analysis. For example, it can be used to create and apply custom measurements, filters, processing and equalization - capabilities that are especially useful when standards are not finalized. MATLAB can also be used to create 2D and 3D data plots derived from measured data.

For additional RF characterization from 10 MHz to 67 GHz, a microwave network analyzer provides single-connection measurements of active devices such as amplifiers, mixers and frequency converters. To simplify test configuration, built-in elements include a second signal source, a combiner and internal signal-routing switches. Example measurements include S-parameters, gain compression, two-tone measurements, and noise-figure measurements on converters and two-port devices. The configuration presented here provides a range of testing and analysis capabilities that address the challenges of developing 802.11ad transmitters and receivers. The suggested combination of flexible software elements and high-performance instrumentation is scalable and reconfigurable to address other technologies as well as future projects. ■

Product News

AdaCore releases GNAT Pro safety-critical for ARM processors

AdaCore announces the availability of its GNAT Pro Safety-Critical product for ARM Cortex micro-controllers. This bareboard GNAT Pro Safety-Critical product provides a complete Ada development environment, oriented towards systems that are safety-critical or have stringent memory constraints. Developers of such systems can now exploit the software engineering benefits of the Ada language, including reliability, maintainability, and portability.

News ID 16936

HCC and Atollic accelerate the debug process for engineers

HCC Embedded and Atollic announced the release of an advanced product that accelerates the debug process for engineers using Atollic's TrueSTUDIO C/C++ IDE and HCC's eTaskSync verifiable task scheduler. Atollic TrueSTUDIO v4.0 was launched at the Embedded World. The TrueSTUDIO debugger will provide kernel aware debugging for HCC's eTaskSync scheduler to give engineers a means to debug embedded systems rapidly. eTaskSync is an advanced kernel that comes with full MISRA-C:2004 compliance, 100% statement/object code coverage and MC/DC analysis.

News ID 16884

ARM announces mbed version 2.0 and open source SDK

ARM unveils the next milestone of the mbed project with a new SDK released under a permissive open source license, a new HDK for creating low-cost development boards. The mbed platform is being developed by ARM to deliver free tools and software that enable effective rapid prototyping with ARM Cortex-M series processor-based MCUs. The mbed SDK, already relied upon by tens of thousands of developers, has been extended and released free under a permissive open source license.

News ID 16898

LDRA tool suite undergoes TÜV SÜD certification for IEC 61508, ISO 26262 and EN 50128

LDRA has started TÜV SÜD review and certification process to verify that the LDRA tool suite is fully qualified to validate software applications for industrial safety (IEC 61508), automotive (ISO 26262), and rail (EN 50128). Validation of full compliance is anticipated by Q2 2013. This TÜV SÜD certification builds on the ISO 9001:2008 certification already achieved by LDRA in its forty year advocacy for better quality software and development.

News ID 16902

Rohde & Schwarz: generation and analysis of WLAN IEEE 802.11ac signals up to 160 MHz

New options extend the baseband of the R&S SMBV100A vector signal generator to 160 MHz, making it the only signal generator to directly support high-speed modes for WLAN IEEE 802.11ac. An external PC is not needed. In the 5 GHz ISM band, the R&S SMBV100A offers exceptional signal performance (0.44 % EVM) for 160 MHz signals. The latest generation of the field-tested R&S FSV signal and spectrum analyzer can also be equipped with a demodulation bandwidth of 160 MHz. Unmatched in the general-purpose instrument class, the analyzer can now be used to record and demodulate a WLAN IEEE 802.11ac signal in its full bandwidth of up to 160 MHz.

News ID 16890

The launch of the new MISRA C: 2012 (MISRA C3) Guidelines

Paul Burden, Senior Technical Consultant and PRQA representative on the MISRA working committee, talked about the new guidelines with ECE Magazine editor Wolfgang Patelay.

ECE: So, Paul, give me a bit of background to MISRA

Burden: The MISRA mission statement speaks of providing assistance to the automotive industry in the application and creation within vehicle systems of safe and reliable software. MISRA has published a variety of documents over the years. It has contributed significantly to developments in functional safety, particularly the ISO 26262 standard, and the development of coding guidelines for C and C++ - MISRA C and MISRA C++. MISRA C was first published in 1998. It provided some badly needed guidance to engineers, often with very limited experience in software engineering, at a time when software reliability was becoming a critical issue. To start with, it was a modest initiative within the UK motor industry, but it rapidly developed into a project of major significance. A second version of MISRA C appeared in 2004, and a third version, MISRA C:2012, was launched on 18 March 2013.

ECE: So how significant is this particular update to the MISRA C coding guidelines?

Burden: A lot of work has gone into the latest version and the result is a better document. MISRA C has a large following and I would expect the new version to be of interest to anyone developing systems in C who cares about software quality.

ECE: But why was it necessary to produce another edition?

Burden: It is not an easy decision to change something that is widely accepted and widely used, so there had to be a good reason to bring out a new version of MISRA C. In fact, there were several key reasons: support for C99, responding to user feedback and an acknowledgement that improvements could be made.

Paul Burden, Senior Technical Consultant and PRQA representative on the MISRA working committee

ECE: Is MISRA C just an automotive standard?

Burden: Not at all. MISRA C is now in use worldwide. It is used in a wide range of different industries – aerospace, defence, medical instruments, process control, nuclear power, consumer electronics and critical systems in finance. It is the most widely used set of coding guidelines for development in the C language.

ECE: So what are the key differences compared to the previous version?

Burden: There are the following five main differences. First the language: C has evolved. Support is now provided for C99 as well as C90. Second the document structure: MISRA C3 includes 16 directives and 143 rules. Compliance with a rule can be determined solely from analysis of the source code. Compliance with a directive may be open to some measure of interpretation or may, for example, require reference to design or requirements documents. Third the deviation classification: Each directive or rule is classified as Mandatory, Required or Advisory.

Deviations are optional for Advisory rules but compulsory for Required rules – as in MISRA C:2004. Mandatory rules may not be deviated – ever! No circumstances are envisaged where it would ever be desirable or necessary to violate these rules. Fourth the analysis scope: Compliance with many rules can be assured by analysis of the code in each translation unit in isolation. Other rules require analysis of all code in the program. Each rule is now classified explicitly as either a single translation unit rule or a system rule. This distinction is important for two reasons.

Firstly because ensuring compliance with system rules requires more extensive analysis; and secondly because some system rules are undecidable. If a rule is undecidable, no tool, however sophisticated, can guarantee to identify every non-compliance. And last but not least fifth the improved rule definition: Rules are now more rigorously defined and better explained.

ECE: What does this mean for legacy code which is already MISRA C:2004 compliant?

Burden: Each version of MISRA C has been larger than the last but the number of rules has not increased greatly. In MISRA C:2012 a few new rules have been added – mainly for C99, and a few have been removed or redrafted. The document is larger, mainly because of many improvements in the explanation and definition of rules. There are new requirements but these are relatively few and code which complies with MISRA C:2004 is likely to comply with MISRA C:2012 with relatively little modification.

ECE: Are there any pre-approved/validated/-certified MISRA C3 checker tools available?

Burden: No, MISRA does not endorse tools or provide certification services. However, TERA-Labs, a division of the University of Antwerp, recently completed a comparative study of 8 MISRA C checking tools. Our product, QA C, was confirmed as the best code analysis tool for enforcing MISRA C2 compliance and we have continued to build on this lead in our enforcement of MISRA C3.

ECE: So are PRQA tools ready to support MISRA C3?

Burden: Yes! We announced at Embedded World availability of our MISRA C:2012 compliance module for QA C and we were ready to start supporting customers as soon as the Guidelines were published. ■

Design reuse – managing data and processes

By Rob Evans, Altium

Design reuse offers many advantages but the problem is guaranteeing the integrity of reusable design data. This article describes a new approach, in which design content is released into a secure storage vault as a unique, traceable revision, also containing any number of child elements such as components and sub-circuits, maintaining integrity down to the lowest level.

In electronics design the need to reuse assets has grown increasingly insistent as product development becomes more complex and project timelines reduce. The efficiency advantages of reduced design time and lower costs, and the potential safety net of harnessing design elements of a known origin and quality, make design reuse a compelling concept. To make practical design reuse a reality one of the key factors, most difficult to achieve, is assuring the integrity of reusable design data – without it, the risk is too high and we don't have the confidence to reuse that design data. Because of that doubt, designers and organizations are understandably reluctant to take the risk of tackling real design reuse at anything but a high-cost enterprise level.

Yet at its most fundamental level, design engineers practice design reuse in every hardware project through the use of integrated circuits – off-the-shelf ICs that have been rigorously tested and used in countless other designs. ICs generally contain a complex collection of circuitry, but we have faith in the integrity of what's inside. This example points to the essential concepts of effective design reuse. Here, the reapplied collection of electronics and data is a known and trusted commodity. There's no need to reinvent the wheel by designing its internal circuitry, since we have full confidence in the integrity of the 'pre-assembled' version. And secondly, we aim for a disciplined approach to establishing, storing and using the design data associated with that reusable element, by rigidly using a formalized source (such as company database libraries) that features standardized naming conventions and data structures. It highlights two clues to practical and effective design reuse – maintaining design data integrity and a disciplined approach to how that data is created and applied.

In practice, the main challenge when reusing components tends to be further down the design path where we commit to the final stages of releasing a design for prototyping or production. At this point we need to be confident that the component data is up-to-date and relevant, or more specifically, that a part is still available, still cost-effective in numbers required, and not superseded by a more suitable component.

Managing the integrity of collections of components – ensuring their reuseability in effect – can take on the form of locally approved component libraries right through to company database libraries that hook into the organization's lifecycle management system. The practical effectiveness of these systems varies widely – higher level, more complex and intrusive data management tends to restrict component choice and is disconnected from the design process, while an informal, local approach carries a higher degree of risk but is an interactive part of the environment where component decisions are actually made.

It's at the highest level of design reuse where things really become challenging and our confidence understandably wanes. The ultimate aim of recycling design resources is the ability to confidently apply whole sections of pre-existing design content in new design projects – reusing our hard-won and painstakingly developed design IP. This is design reuse at a much higher level of abstraction, where the number of elements and variables included in each saved design package can be huge. Here, each reusable section will represent the circuitry and sub-elements – components (including models and parameters), nested circuitry and so on – that are needed to deliver the function of that package.

To date, this level of design reuse has been tackled using an ad hoc approach based on copy-and-paste techniques, or at best, a system to formally store reusable chunks of circuitry. This notional design reuse capability provides the basic mechanisms to implement reusable elements, but does very little (or nothing at all) to mitigate the risk of using them. You just can't be sure that the source circuitry is the latest version, its functionality is still viable, it

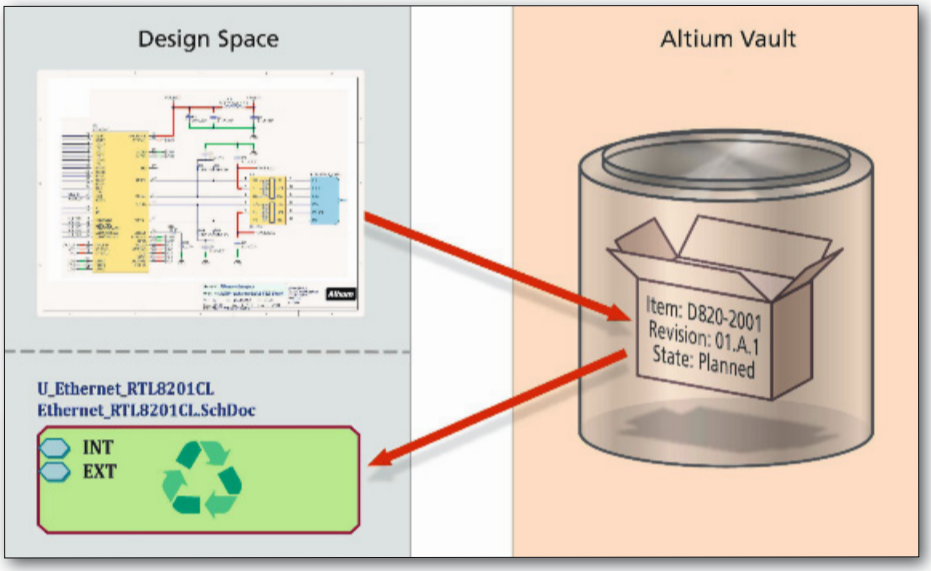


Figure 1. Formally storing a circuit diagram in a fully managed Vault allows its reuse in other design projects that call for the same functionality. This applies to models of individual components just as well as entire electronic devices.

does not contain errors or undocumented modifications, or for that matter, if the components are still suitable, available and cost-effective. The risks of reusing design sections in this way are cumulative and untenable, so providing the design system features and functions needed to reuse design content is of little value when the integrity of that content is in doubt.

What's needed is a practical and effective way to securely store, share and manage locked revisions of reusable design content, then manage the lifecycle of that content to define its suitability for new designs. It involves separating released design data from the fluidity of the design environment into its own fully managed, but accessible, repository. Taking this approach, design content can be released from the design space itself into a secure storage vault as a unique, traceable revision, which can contain any number of child elements (components, sub-circuits, etc). The child content will also exist in the vault as its own set of managed revisions, so the integrity of the parent content is maintained down to the lowest level.

A design section is released into the vault as a reusable schematic sheet (or tree of sheets) and stored as a fixed revision, where its lifecycle status (prototype or production, for example) can be defined over time. If the design source documents are updated, a new sequentially-named revision can be released to the vault and its status set accordingly. A sheet of design circuitry can be formally released into the vault, and then be reused in other design projects requiring that same functionality. In the same way, components released to the vault can be fully managed as revisions, and incorporate links to real-time supplier data that provides up-to-date pricing and availability information. It means that released design packages, and components, exist in a locked and traceable form within the vault, where they can be managed and reused with accurate and up-to-date knowledge of their origin, history and lifecycle state – in effect, their validity for new designs.

Furthermore, once all released items exist in the vault, including full designs released for prototyping or production, the inter-relationships are easy to monitor and track. You can then have an immediate view of what model revisions are used in a component, what component revisions are used in a sheet, what design sheet revision is used in a released design, and so on. When you choose a reusable vault item for a new design, you'll have a full understanding of where it's been used, as well as its origins and current lifecycle status.

Based on server technology, the managed vault system exists separately from the own project data storage of the design system, but can be accessed easily through the design environment itself or from the broader organization. This provides secure, permission-based access to others in the organization such as procurement, manufacturing and administration. Component choices, for example, can then become a cooperative process with purchasing, and vault-based design resource data can be easily accessed by company data management systems.

From a design reuse view it means that all reusable items have a high degree of data integrity. You can be sure that an item is the latest revision, you know it has not changed since it was released into the vault, and you

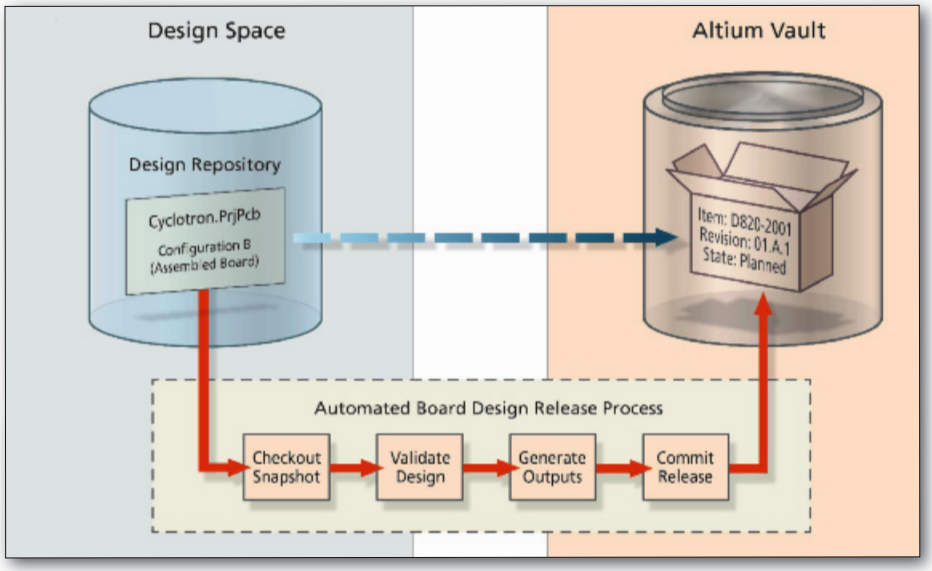


Figure 2. An automated design release process validates a printed circuit board design, which is stored (as revision) in a secure vault where its life cycle status can be managed.

can see where it's used in other design resources. The lifecycle status (prototype, production, etc) sets the reusable item's approval state and how it can be used, and it's clear when a sub-item (such as a constituent component) is no longer approved.

Enabled by the described vault technology, the capability to store, manage and recycle high-integrity design IP brings meaningful design reuse to electronics engineers with the right tools and systems. A unified electronics design system with powerful data management tools can connect directly to the managed vault system for easy design data access and management, allowing verified, tracked design elements and sections of circuitry to be dropped into new designs at will. With all the systems and tools in place, this then opens the opportunity to practise design for reuse (as opposed to design reuse) at a fundamental level. The difference here is that all elements of design are captured and configured so that they can be easily re-used across any new future designs. From components (and their constituent models and data), to sheets of schematic circuitry and up to fully released modular designs, all are released into a vault to essentially create a repository of managed design building blocks. And this is where the process discipline needs to be applied, based on the commitment to a design for reuse approach. From the ground up, standardized naming systems, data storage structures and design methodology need to be instigated (and rigorously applied) to bring order and integrity to the design process, which is based around a common set of secure, lifecycle- managed vaults. The vaults become the essential source for released design data IP, from the lowest component models to complete assemblies ready for production – even newly created design elements are released to the vault so they can be sourced back into a design. The benefits of this defined and structured approach, based around managed vaults and advanced design data management, are substantial and self-perpetuating. Design productivity ramps up as more design content is created, released to and subsequently approved for reuse from the vault. Future designs become quicker to implement as the vault-based repository of design building blocks grows, and required circuit functionality becomes available for placement in a higher-abstracted modular fashion.

Ultimately, the concept of releasing design elements to a fully managed vault provides a robust system for implementing a design for reuse methodology. And it goes way beyond simply providing the mechanisms to access predefined design elements. By addressing the key issues of managing data integrity and implementing a disciplined design methodology and structure, the approach eliminates the risks associated with reusing even high level, multi-layered design sections.

In practice it means that valuable design IP can, and should, be reused with full confidence in its integrity. Implementing design reuse during electronic product development is no longer an act of blind faith or risky bravado – you can now know everything about the content and viability of a reusable element, and most importantly, know that its veracity is assured. And above all, implementing a design for reuse methodology dictates a shift in thinking and approach. Design reuse moves from being a desired bonus, or addition to electronics design, to become the core of how you design, based around fully managed vaults. ■

Product News

JTAG: low-cost boundary-scan suite covers all applications

JTAGLive Studio is a comprehensive package of JTAG/boundary-scan tools that enable designers and manufacturing test engineers alike to develop complete test and programming applications at a low price level. The benefits offered by the JTAG Technology for debugging, testing and in-system programming are not limited to complex designs with many JTAG devices. Designs with only a few, even just one or two, JTAG devices can also greatly benefit from this technology during all stages of the life cycle. A toolset capable of handling even the most (very) complex boundary-scan designs, however, often is not economically feasible for a company that only uses a few JTAG devices in its designs.

News ID 16889

ADI: simulation tool eases development of RF systems

Analog Devices released a new version of its popular ADIsimRF design tool. The free design tool is the software accompaniment to ADI's complete portfolio of RF-to-digital functional blocks, allowing engineers to model RF signal chains using devices from across ADI's RF IC and data converter portfolio. ADIsimRF Version 1.7 adds a number of new device models along with enhanced support for inter-stage mismatch calculations. The design tool provides calculations for the most important parameters within an RF signal chain, including cascaded gain, noise figure, IP3, P1dB, and total power consumption.

News ID 16894

PRQA: sophisticated and collaborative code inspections

PRQA announces a significant upgrade to QA•Verify quality management solution. QA•Verify already leverages the broad industry adoption of QA•C and QA•C++, providing team-sharing collaboration, sophisticated coding standards compliance, metrics and reporting facilities across multiple software projects. The adoption of structured code inspections remains surprisingly low, despite the fact that the benefits are well documented and compelling. Inspections have historically been a manual and intensive effort, difficult to scale as code volume and complexity increases, along with the inevitable schedule and resourcing pressures on a development team's most experienced resources.

News ID 16919

Safer household appliances with low-cost ARM Cortex-M based MCUs

By Vincent Onde, STMicroelectronics

Hardware parity check adoption in the embedded market for general purpose MCUs, combined with an ever-increasing number of system monitoring and safety features, makes applications simpler to be certified, safety-related development tasks easier to be implemented, and most important, makes household appliances safer.

Since 2007, household appliance manufacturers have had to adhere to the IEC60335 safety standard for all new designs. This standard covers everything from mechanical systems to embedded electronics to ensure the equipment is safe and reliable, and more specifically, that a failure will not present a safety hazard to the user.

The electronics section refers to another standard, the IEC60730, which covers automatic electronic control for a wide range of applications. In particular, Annex H is important for embedded systems developers since it focuses on programmable devices. Microcontrollers are common in white goods, often used in multiples: typically, one manages the dashboard while another one handles valve and motor control.

The standard distinguishes three software classes, A, B and C, depending on the danger a piece of equipment presents if it fails. If the safety of the appliance does not rely on software, it falls into Class A - room thermostats or lighting controls, for example. At the opposite end of the spectrum, if the software is intended to prevent special hazards such as an explosion in electronically-fired gas burners, it is evaluated as Class C. Class C is not covered in this article since most household appliances whose electronic controls must prevent unsafe operation belong to Class B. Class B includes washing machines for example, with the potential issues related to electronically controlled door locks or to thermal cut-offs of motors. The IEC60730 table H.11.12.7 in Annex H lists the microcontroller components to be tested, the faults to be detected, and the acceptable measures, for both software class B and C. It includes the CPU (registers and program counter), interrupts (handling and execution), clock frequency monitoring, checks on variable memory (RAM) and invariable memory (flash, EEPROM), external communications, and peripherals. These checks are first done exhaustively during the MCU boot, even before the system start-up code execution takes place. Why? The main reason is that the RAM test is 'destructive' and would corrupt the initialized variables.

What is asked for within a RAM check? For Class B, the standard requires single-bit DC fault detection (for instance stuck-at or coupling fault) to be done periodically. Since most of the entry-level MCUs do not have parity bits included in their SRAM, the test must be implemented by software. March algorithms detect these faults with a limited number of passes: March C- fits perfectly (using 10.n operations, n being the number of locations to be tested) but March X (6.n operations) is also accepted by test institutes in particular cases. Once the test is complete, the RAM memory is erased (thus the term 'destructive test'). Carrying out a March test following the reset does not present particular difficulties. It has no real drawback other than slowing down the start-up procedure a little bit: given the small quantity of embedded SRAM, usually this is not even noticeable. On the other hand, it can be quite a challenge if repeated during run-time.

Firstly, it must be made transparent: the application must handle the RAM without particular protocol, as if the test were not implemented. Practically speaking, this imposes the following conditions. It must be implemented in an interrupt service routine (ISR), served with the highest priority. This guarantees the data will not be accessed by the application while testing is done. A memory buffer must be provisioned, so that the content of the RAM area being checked can first be backed up and finally restored before resuming the applicative tasks. Obviously, this buffer must also be periodically verified.

Secondly, it must not suspend the application for too much time. The check is usually split in a number of partial tests to limit the time spent in this top level task. Still, the number of locations tested at once cannot be lower than 3 consecutive locations (this is mandatory to have coupling fault coverage), which represents no less than 30 successive read/write accesses using a March C- algorithm. Although

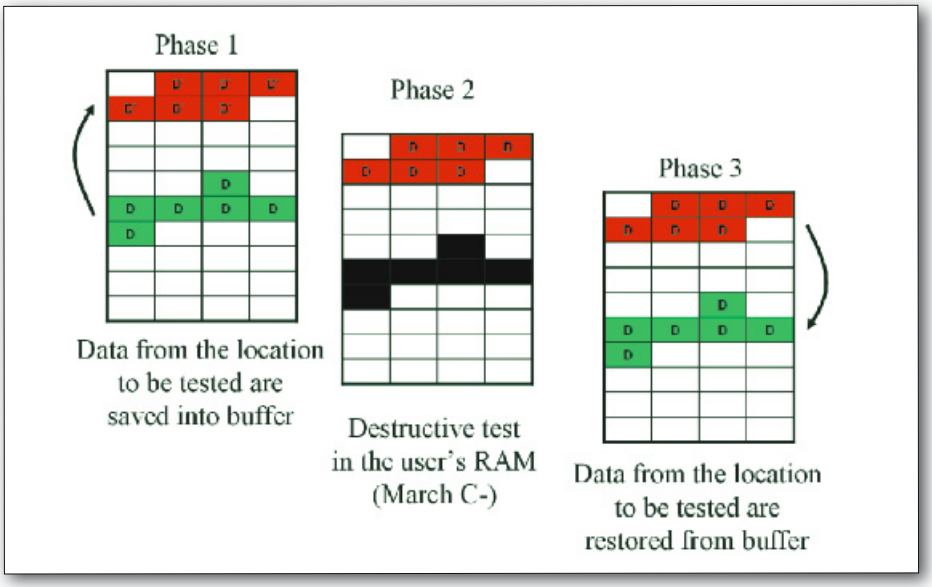


Figure 1. Software for handling the partial RAM test during run-time

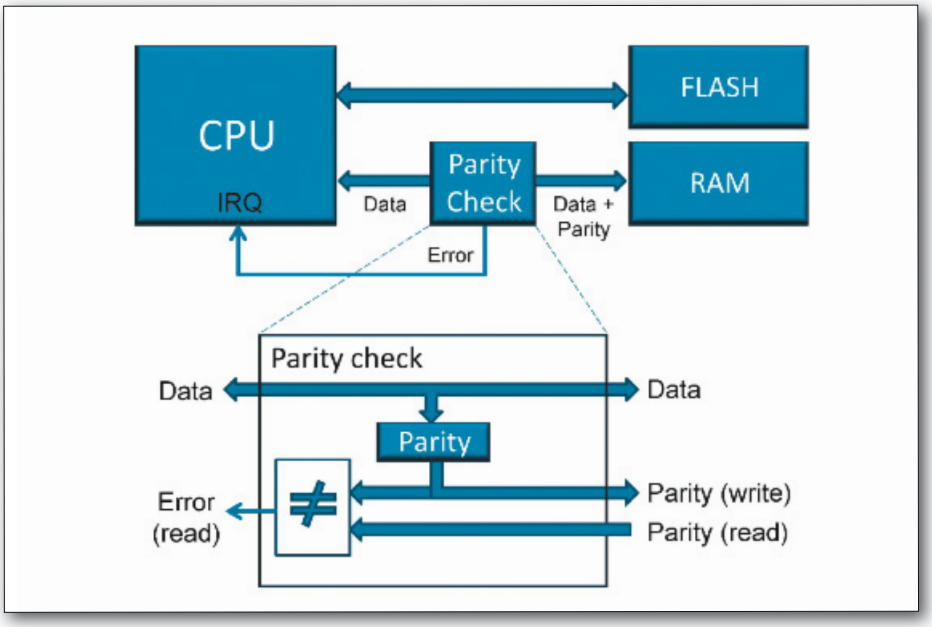


Figure 2. When the data is read, its parity is computed and checked against the reference value.

this solution has proven to be effective and is nowadays a common industry practice, it has a number of drawbacks. Let's consider it from the software engineering standpoint first. We will not review the benefits of structured programming, but let's look at the constraints related to this implementation. Encapsulation issues: the C modules must have part of their internal variables promoted as global and thus no longer subject to the sanity checks done by the compiler against cross modules accesses. Low tasks isolation and poor modularization: the test structure imposes a test access to each safety critical software module and makes the addition of new features more complex. We can also consider potentially higher risks of data corruption if we link its probability to the number of read/write accesses. This is mitigated by inverse redundant storage of safety critical variables, but this in turn increases the size of the area to be "Class B tested".

From the MCU resources standpoint, the test implementation consumes ROM and RAM, as well as CPU bandwidth: if the core is temporarily unable to absorb the test burden on top of its regular processing task, the test might have to be stopped during a computationally critical operating phase of the appliance. Finally, a run-time RAM check affects real-time responsiveness (it can delay or even suspend any other ISR) and can conflict with low-latency or emergency tasks requirements. The length of the test routine cannot be minimized: a minimum number of consecutive memory locations must be evaluated for coupling faults coverage. And the complexity increases if the software has to manage address descrambling to be in line with the physical memory layout. How software handles the partial RAM test during run-time is shown in figure 1. The IEC60730 standard proposes an alternative solution consisting of a hardware parity bit. Although this is standard procedure for DRAM memories, this is quite unusual in general purpose microcontrollers; advanced silicon process nodes have made such features more cost-effective. The solution consists of adding one parity bit per memory location: the parity is computed at the time the memory is written and stored in parallel with the data. When the data is read, its parity is computed and checked against the reference value, as represented in figure 2. In case of a difference, either due to data or parity bit corruption, an interrupt or exception signal line is asserted.

The core then handles the error in a dedicated safety ISR and shuts down the appliance properly. In a second step, the core may re-start the application (hot reset) or definitively stop the equipment with a maintenance code displayed. The benefits of this implementation are obvious. Class B RAM check is made completely transparent: Software practices do not need to be compromised, no MCU vendor specific test routine has to be developed, other than a global fault handling function which must be present in any case, no specific RAM partitioning and linker script is needed, CPU bandwidth is fully available for the application (the parity computation does not increase the memory reading latency), and real-time behavior is optimum. As a final benefit, this eliminates the need for the full RAM check at start-up and lowers the boot time, since the parity check is active right after the power-on reset.

Brushless motors are used in appliances because of their high efficiency, silent operation and robustness, but complex control and dedicated PWM peripherals are necessary. Particular care is needed for fault protection and safe shut-down. For this purpose, the RAM parity error checking mechanism improves reliability and response time. Rather than managing safe shut-down by software, the parity error signal is directly routed to the PWM peripherals to trigger an emergency shut-down automatically and avoid system clock and software-related delay. The block diagram in figure 3 presents a practical implementation.

Care must also be taken to monitor other critical system parameters. A power supply monitoring system can be programmed to issue an interrupt if the Vdd voltage drops below a pre-programmed value. Similarly, a clock security system verifies that the main clock is operating properly and issues an interrupt in case of ab-

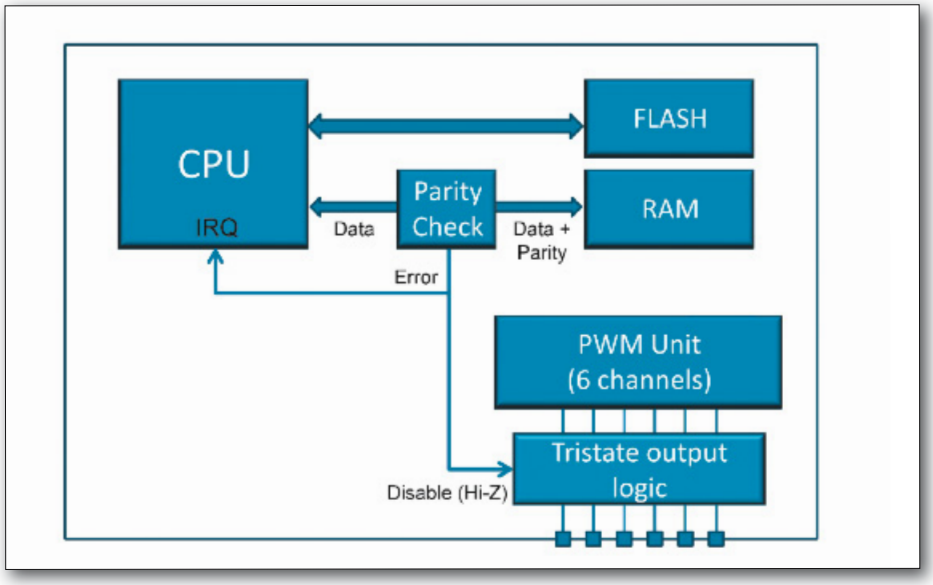


Figure 3. Block diagram of a practical implementation

normal operation. Additionally, the Cortex core provides a signal at the chip level to indicate when the core enters lockup state, which can take place when a fault occurs inside the hard fault or the NMI handlers, or when a bus fault occurs during the boot sequence. These three events, together with the parity, are merged for asserting an internal emergency shutdown signal, which is itself OR'ed with the external break input. A failsafe clock circuitry is also required by the norm. This is partly achieved using a clock security system peripheral (CSS) that automatically switches the main clock back to an internal high-speed oscillator in case of crystal failure. Additionally, it is necessary to provide a means to monitor the external clock by comparing the expected external frequency with an internal one. The real-time clock timer can be supplied by the LSI (low speed internal) internal RC oscillator to measure the main system clock precisely enough to detect a 50% change due to operation on the crystal sub-harmonics. At system level, this can save the cost of circuitry able to do 50/60Hz mains zero-crossing detection. The norm proposes an independent time-slot monitoring to prevent any CPU run-away in case of a program counter malfunction: this is the duty of the watchdog timer, which is embedded in most MCUs. Nonetheless, it is stated that it must be fully independent. For this reason, the STMicroelectronics Cortex-M based STM32 family has two watchdogs: a regular window watchdog running on the main clock source, and a second watchdog, using an independent internal oscillator and started with an option byte located in flash memory. This ensures that at least one watchdog will be active in case of crystal failure and whatever the clock circuitry configuration.

Finally, the MCU embeds a 32-bit hardware CRC calculation unit, which significantly speeds-up the flash content integrity check and reduces the related CPU load (spend during run-time) to a negligible value. This peripheral can even be fed by the DMA controller. It gives the possibility to have the flash integrity check done as a background task during run-time. ■

Product News

■ **Infineon: easy switch from 8-bit to 32-bit with XMC1000 Industrial MCUs**

At Embedded World, Infineon Technologies presented samples of its new XMC1000 industrial 32-bit microcontroller family which provides system designers with strong incentive to switch from 8 to 32 bit MCU architecture. With XMC1000, Infineon offers a fully-featured 32-bit alternative for hitherto 8-bit users by combining the ARM Cortex-M0 processor core with powerful peripherals, high productivity design tools and costs typical of 8-bit devices based on production using state-of-the-art, 65nm embedded Flash technology on 300mm wafers.

News ID 16910

■ **Holtek: Tinypower MCU for 3D Glasses comes in 16-pin SSOP package**

Holtek's new HT45FH3T MCU comes fully integrated with the necessary high voltage circuits which are a requirement for 3D Glasses applications. In addition to including all the original functions of the previous HT45F3T, this new device also includes a 3V low dropout voltage regulator and four level shift functions. These features extensively reduce the need for peripheral components, resulting not only in reduced cost but also reduced PCB areas.

News ID 16988

PRQA announces support for MISRA C:2012

PRQA announces that its tools offer support for MISRA C:2012 (MISRA C3), with an updated compliance module for QA•C Version 8.1, in anticipation of the new version of the coding standard which will be published on 18 March. The new standard contains a number of improvements over previous versions and extends support to the C99 version of the C language (ISO/IEC 9899:1999).

News ID 16912

Freescale and ARM extend relationship with Cortex-A50 processor license

Freescale is licensing the ARM Cortex-A50 series of microprocessors for future versions of its i.MX applications processor and QorIQ communications processor product lines. This agreement is part of a new multiyear subscription license with ARM that demonstrates Freescale's commitment to the ARM architecture and its intent to further expand its ARM Powered portfolio – one of the industry's broadest range of solutions built on ARM technology.

News ID 16938

AdaCore and Wind River to offer joint product training services in Europe

AdaCore together with Wind River announced the availability of joint education and mentoring services in Europe. A natural extension to an already successful technology partnership, specialized training courses will allow customers to enhance the efficiency of their embedded system development.

News ID 16924

Express Logic and Cypherbridge team on secure cloud device kit

Express Logic and Cypherbridge Systems announce the integration of the Cypherbridge embedded secure Cloud Device Kit for Express Logic platforms. This integrated solution enables embedded devices to connect securely to the cloud using JSON and XMPP. The solution is targeted at vertical markets including grid, commercial and residential energy management, M2M, telemetry, metering, SCADA, payment, and gaming terminals.

News ID 16895

Rohde & Schwarz: analyzing power supply units

The R&S RTO and R&S RTM oscilloscopes from Rohde & Schwarz are the right tools for analyzing power supply units. The frontends of both instruments have outstanding features offering clear advantages over other solutions. Their high dynamic range allows for precise characterization of the power on operations of an embedded system. Power analysis requires that users measure voltage and current.

News ID 16913

Elektrobit provides development platform for Renesas' infotainment system

The runtime solution of Elektrobit's development platform for human machine interfaces, EB GUIDE Graphic Target Framework, has been ported to the Renesas' R-Car H1. This is the latest member of the R-Car series of automotive SoCs. The collaboration will enable car manufacturers to use the high-end Renesas chip in combination with the EB GUIDE GTF to utilize the advanced graphical capabilities of the SoC. The carmakers will benefit by a huge acceleration in development processes and will also be able to create cost effective prototypes of future HMI platforms.

News ID 16939

IAR: Embedded Workbench for STM8 adds new text editor and source browser

IAR Systems launches a new version of its development tools for STMicroelectronics' STM8. The new version 1.40 of IAR Embedded Workbench for STM8 adds user-friendly functionality in the form of a new text editor and source browser, integration with the version control system Subversion and new license management features. Also added is support for additional devices and a new debugging guide.

News ID 17014

Berner & Mattner: improved change management for IBM Rational Statemate models

Berner & Mattner's new PowerDiff version 9.1 facilitates the development of complex systems with IBM Rational Statemate. PowerDiff is the only graphical diff tool for IBM Rational Statemate models and ensures model consistency as well as traceability of changes during the system's entire life cycle. The new version for Windows XP and Windows 7 provides users of the defence, aeronautics and automotive industries with an improved graphical user interface and additional extended functions.

News ID 16880

Enea Linux supports Xilinx Zynq-7000 All Programmable SoC

Enea Linux is now available for the Xilinx Zynq-7000 All Programmable SoC family, providing a comprehensive cross-development tool chain and runtime environment that may be combined with Enea and other proprietary technologies, depending on the specific use cases and requirements. The Zynq-7000 devices combine the software programmability of an ARM Cortex-A9 MPCore with the hardware programmability of an FPGA, resulting in unrivaled levels of system performance, flexibility, and scalability while providing system benefits in terms of power reduction and lower cost with fast time to market.

News ID 16953

Advertisers Index

LieberLieber: C-Code generator and graphical debugger for UML

LieberLieber will provide a graphical UML debugger for the development of embedded systems integrated in Enterprise Architect of Sparx Systems. The code generation engine UML2C generates simple and target independent ANSI C-code for State Machines and Activity Diagrams. The compiled code can be directly flashed into the target device. Finally, LieberLieber`s Enterprise Architect Add-On AMUSE Embedded will be able to connect to the device and allow for graphically testing and model debugging.

News ID 17015

Swissbit and HCC demonstrate fail-safe embedded storage system

Swissbit and HCC Embedded will demonstrated a completely robust, fail-safe embedded storage system at the Embedded World. The system is based on a combination of Swissbit's Industrial SD Card and HCC's SafeFAT fail-safe file system. In order to achieve a truly fail-safe storage system, the behavior and requirements of all layers of the system must be properly defined. The demonstration will use Swissbit's S-200 Industrial SD Card, with intelligent power-fail protection and recovery, in conjunction with HCC's fail-safe SafeFAT file system.

News ID 16887

MSC: 16 kbit FRAM in space-saving SON-8 package

MSC now offers the addition of a new smaller package to the MB85RC16, 16 Kbit Ferroelectric Random Access Memory, from Fujitsu Semiconductor Europe. The new 16 kbit FRAM features ultra low-power consumption. The package dimension of the MB85RC16 is just 3 mm x 2 mm. Compared with the older SOP-8 package, the new SON-8 package reduces the mounting space by up to 80 percent.

News ID 16882

Toshiba: structured ASICs for European customers

Toshiba Electronics Europe has announced the European availability of a Structured Array technology. The technology provides an ASIC alternative to FPGA with lower cost and power consumption - but still at significantly lower implementation and sample/production turn-around time than standard ASICs. Based on technology licensed from BaySand, Toshiba's Structured Arrays support the rapid creation of high-performance, low-power SoC devices.

News ID 16999

Altera to build next-generation FPGAs on Intel's 14 nm tri-gate technology

Altera and Intel Corporation announced that the companies have entered into an agreement for the future manufacture of Altera FPGAs on Intel's 14 nm tri-gate transistor technology. These next-generation products, which target ultra high-performance systems for military, wireline communications, cloud networking, and compute and storage applications, will enable breakthrough levels of performance and power efficiencies not otherwise possible.

News ID 16978

Mouser and Altera sign worldwide distribution agreement

Mouser Electronics announced the signing of a worldwide distribution agreement with Altera. Through this agreement, Mouser becomes an authorized global distributor of Altera FPGAs, CPLDs, development tools, intellectual property cores and development kits. Mouser gives design engineers fast, easy access to the widest range of semiconductor technologies.

News ID 16932

ADI: prototyping kit simplifies A/D converter-to-FPGA connectivity

Analog Devices unveiled the newest addition to its line of FPGA development platform-compatible FPGA mezzanine cards incorporating JEDEC JESD204B SerDes technology. Digital and analog designers can use the AD9250-FMC-250EBZ kit to simplify and rapidly prototype high-speed JESD204B A/D converter-to-FPGA platforms. The AD9250-FMC-250EBZ features two AD9250 dual 14-bit high-speed JESD204B data converters providing four 14-bit A/D converter channels at 250 MSPS in an FMC-compliant form factor.

News ID 16906

Reflex CES: 25-million gates or more ASIC prototyping platform with partitioning software

Reflex CES introduced FPP25, a fast ASIC/SOC prototyping platform for emulating designs of up to 25-million ASIC gates using a stand-alone system. Based on Xilinx Virtex-7 2000T FPGAs, FPP25 exploits Reflex CES' collaboration with Flexras and Adacsys, to offer design engineers an easy-to-use, next generation platform to speed up validation and verification of complex, high density digital designs.

News ID 16927

MEAS: 1.8 V digital humidity sensor in a small package

Measurement Specialties now offers the HTU21D, a compact, low power digital humidity/temperature sensor. The self-contained sensor interfaces directly with a micro-controller ensuring a better signal path as well as reducing costs, space requirements and power consumption. The HTU21D, which requires only 1.8 V for operation, offers an adjustable resolution for humidity and temperature of 8/12-bit or 12/14-bit, depending on needed response time.

News ID 16970

Rohm: dedicated PMIC to support "Bay Trail" platform

ROHM has announced the development of a dedicated system power management IC to support Intel's latest Atom-based platform, code name "Bay Trail". A highly integrated power management solution with industry leading power efficiency, ROHM's PMIC is targeted towards ultra-thin form factor tablet and convertible devices.

News ID 16967

Silica: ArchiTech initiative for design and development tools

SILICA has launched a major engineering support initiative called ArchiTech. With ArchiTech, the semiconductor distributor aims at providing a full solution and single-point-of-contact for all requirements related to design tools. ArchiTech solutions will help customers to bring new designs to market on time and in the most efficient possible way. The distributor brings together robust development tools, engineering and software expertise, in-depth training and extensive documentation.

News ID 16955

GOEPEL upgrades ChipVORX for Bit Error Rate Tests

GOEPEL electronic's IP-based ChipVORX technology has been extended to execute Bit Error Rate Tests (BERT). The highly automated solution enables FPGA Embedded Instruments utilization in the form of special softcores for the test and design validation of high-speed I/O. Users can now evaluate the transmission channel quality via measurement of the bit error rate. A graphical evaluation via eye diagram is possible to support design validation.

News ID 17017

ECE

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ARM-based Embedded System Design

June 25, 2013 - Sindelfingen/Germany

ARM-based systems are rapidly gaining popularity in the Embedded Market. This one-day conference with table-top exhibition aims to provide a comprehensive overview about new products, technologies and strategies for ARM-based Embedded System Design.

- ARM architectures: overview and outlook
- ARM-based microcontrollers & processors
- ARM-based boards & modules
- Software support & development tools

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Conference Programme

Keynote 1 – Technical Trends & Future Outlook
presented by ARM, length 40 minutes

Keynote 2 – Software Support for ARM
presented by Carsten Emde (OSADL), length 30 minutes

Panel
During the panel, major Board, Chip and Software companies explain their ARM strategy and give a short preview of the papers in the afternoon conference tracks.

Conference Track 1 – Chips & Tools
Products & Technologies Sessions

- Microprocessors & Microcontrollers
- Development Tools for ARM Architecture
- ARM-based FPGAs and SoCs

Conference Track 2 - Software & Services
Products & Technologies Session

- RTOS, Middleware, Application Software, ...
- Software and Services for ARM-based Systems Design

Conference Track 3 – Boards & Modules
Products & Technologies Session

- ARM-based Boards, Modules & Systems

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