Gen 2 SiC MOSFETs Extends the Benefits of Silicon Carbide in Industrial Applications

Dr. Vladimir Scarpa, Salvatore La Mantia
Michele Macauda, Luigi Abbatelli
• Silicon Carbide at STMicroelectronics
• SiC MOSFET - Technology roadmap
• Gen 2 SiC MOS Technology
• STGAP2S Isolated Gate Driver
• Practical Example
Contents

• Silicon Carbide at STMicroelectronics
• SiC MOSFET - Technology roadmap
• Gen 2 SiC MOS Technology
• STGAP2S Isolated Gate Driver
• Practical Example
20 Years of ST SiC History

April 1998
1st contract on SiC with CNR-IMETEM (Dr. V. Raineri)

November 2003
First ST internal product request

February 2003
ETC Epitaxial reactor prototype installed in ST

May 2002
Schottky Diode Demonstrator (CNR line)

December 2005
Schottky Diode Mat 20

June 1996
Collaboration with Physics Dept. (Prof. G. Foti)

May 2004
Schottky Diode Demonstrator (ST line)

October 2007
1st Gen Diode Start Production

November 2003
First ST internal product request

October 2007
1st Gen Diode Start Production

May 2004
Schottky Diode Demonstrator (ST line)

May 2004
Schottky Diode Demonstrator (ST line)

December 2005
Schottky Diode Mat 20

May 2009
Power MOSFET 3” Demonstrator

September 2009
1st Gen MOSFET Start Production

February 2003
ETC Epitaxial reactor prototype installed in ST

October 2007
1st Gen Diode Start Production

September 2003
1.2kV Diode Start Production

May 2004
Schottky Diode Demonstrator (ST line)

May 2012
2nd Gen Diode Start Production

June 2003
2" ST line

June 2006
3" ST line

June 2011
4" ST line

June 2016
6" ST line

Pioneers...

September 2013
3rd Gen 3 Diode Start Production

June 2014
2nd Gen MOSFET AG 6" Start Production

June 2017
2nd Gen MOSFET AG 6" Start Production

June 2016
6" ST line

...to mass production
ST SiC Manufacturing

Silicon Carbide manufacturing line growth

Normalized to capacity in 2017

Catania 6” wafer size capacity evolution
• Silicon Carbide at STMicroelectronics
• SiC MOSFET - Technology roadmap
• Gen 2 SiC MOS Technology
• STGAP2S Isolated Gate Driver
• Practical Example
SiC MOSFET Technology RoadMAP

From Planar to Trench

$R_{sp}$ (mOhm*cm$^2$)

- Planar
- Trench

1.2kV

-44%

650V

-28%

-30%

In Production

- Gen 1
  - Driving Voltage: 20V

New!

- Gen 2
  - Driving Voltage: 18V

In Development

- Gen 3
  - Driving Voltage: 18V
- Gen 4
  - Driving Voltage: 15V

New! In Production In Development
SiC MOSFET Benchmark
Parameter: $R_{DS,ON} \times \text{Area}$

- **Gen1 (2014)**
- **Gen2 (2018)**
- **Gen3 (2020+)**

- **Comp. 1**
- **Comp. 2**
- **Comp. 3**

- **Trench technology**

✓ ST Gen2 as good as today’s Trench MOSFETs
• Silicon Carbide at STMicroelectronics
• SiC MOSFET - Technology roadmap
• Gen 2 SiC MOS Technology
• STGAP2S Isolated Gate Driver
• Practical Example
## SiC MOSFET Gen 2 – Planned Portfolio

<table>
<thead>
<tr>
<th>$V_{ds}$ [V]</th>
<th>$R_{ds(on)}$ typ @ 18V, 25°C [mΩ]</th>
<th>Id</th>
<th>Package</th>
<th>P/N</th>
</tr>
</thead>
<tbody>
<tr>
<td>650</td>
<td>18</td>
<td>90</td>
<td>HiP247, H2PAK-7, HiP247-4L</td>
<td>SCTW90N65G2V, SCTH90N65G2V-7, SCTW90N65G2V-4</td>
</tr>
<tr>
<td></td>
<td>23</td>
<td>100</td>
<td>HiP247, H2PAK-7, HiP247</td>
<td>SCTH100N65G2-7AG, SCTW100N65G2AG, SCT100N65G2D2AG</td>
</tr>
<tr>
<td></td>
<td>55</td>
<td>45</td>
<td>HiP247, H2PAK-7</td>
<td>SCTH35N65G2V-7AG</td>
</tr>
<tr>
<td></td>
<td>55</td>
<td>45</td>
<td>HiP247, H2PAK-7, HiP247-4</td>
<td>SCTW35N65G2V, SCTH35N65G2V-7, SCTW35N65G2V-4</td>
</tr>
<tr>
<td>1200</td>
<td>25</td>
<td>80</td>
<td>HiP247, H2PAK-7</td>
<td>SCTW70N120G2V, SCTW70N120G2V-4, SCTH70N120G2V-7</td>
</tr>
<tr>
<td></td>
<td>30</td>
<td>80</td>
<td>HiP247, H2PAK-7, HiP247</td>
<td>SCTH100N120G2-AG, SCTW100N120G2AG, SCT100N120G2D2AG</td>
</tr>
<tr>
<td></td>
<td>70</td>
<td>45</td>
<td>HiP247, H2PAK-7</td>
<td>SCTW40N120G2V, SCTH40N120G2V-7</td>
</tr>
<tr>
<td></td>
<td>75</td>
<td>40</td>
<td>HiP247, H2PAK-7</td>
<td>SCTH40N120G2V7AG, SCTW40N120G2VAG</td>
</tr>
</tbody>
</table>

### Packages

- **SMD**
  - Kelvin Source + $T_{j,max}=200°C$
  - H2PAK 2 and 7 leads

- **TO247.4**

### Values

<table>
<thead>
<tr>
<th>$V_{ds}$ [V]</th>
<th>$R_{ds(on)}$ @ 25°C [mΩ]</th>
<th>Id</th>
<th>P/N</th>
</tr>
</thead>
<tbody>
<tr>
<td>650</td>
<td>55</td>
<td>50</td>
<td>SCTW35N65G2V-4</td>
</tr>
<tr>
<td></td>
<td>18</td>
<td>110</td>
<td>SCTW90N65G2V-4</td>
</tr>
<tr>
<td>1200</td>
<td>25</td>
<td>90</td>
<td>SCTW70N120G2V-4</td>
</tr>
</tbody>
</table>
SiC MOSFETs Qualification Status

<table>
<thead>
<tr>
<th>Test</th>
<th>PC</th>
<th>Std ref.</th>
<th>Stress Conditions</th>
<th>Duration</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>Die Oriented Tests</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HTRB</td>
<td>N</td>
<td>JESD22 A108</td>
<td>Tj = 200°C, BIAS = 960V</td>
<td>1000 H</td>
<td>Pass</td>
</tr>
<tr>
<td>HTGB</td>
<td>N</td>
<td>JESD22 A108</td>
<td>Tj = 200°C, BIAS = +22V</td>
<td>1000 H</td>
<td>Pass</td>
</tr>
<tr>
<td>HTSL</td>
<td>N</td>
<td>JESD22 A-103</td>
<td>TA = 200°C</td>
<td>1000 H</td>
<td>Pass</td>
</tr>
<tr>
<td>Package Oriented Tests</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>AC</td>
<td>N</td>
<td>JESD22 A-102</td>
<td>Pa=2Atm / TA=121°C</td>
<td>96 H</td>
<td>Pass</td>
</tr>
<tr>
<td>TC</td>
<td>N</td>
<td>JESD22 A-104</td>
<td>TA = -65°C to 150°C</td>
<td>500 cy</td>
<td>Pass</td>
</tr>
<tr>
<td>TF/IOL</td>
<td>N</td>
<td>Mil-Std 750D Method 1037</td>
<td>ΔTC ≥ 105°C</td>
<td>10Kcy</td>
<td>Pass</td>
</tr>
<tr>
<td>H3TRB</td>
<td>N</td>
<td>JESD22 A-101</td>
<td>TA=85°C , RH=85% , BIAS= 100V</td>
<td>1000 H</td>
<td>Pass</td>
</tr>
</tbody>
</table>

- Same qualification path than Silicon parts;
- Temperature increased to Tj=200°C for HiP247 Package
Advantages – Static Parameters

Low temperature dependency of $R_{ds,\text{on}}$

- Lowest temperature dependency among SiC MOSFETs in the market;
- Lower risk of thermal runaway even at very high temperature operation.
Relevant Parameters for Safe Gate Driving

1) Miller Capacitance

- Weak capacitive coupling through Miller Capacitance.
- Low risk of parasitic turn-on.
- Operation inside SOA, no gate oxide degradation.

\[ \begin{align*}
C_{\text{rss}} &= C_{GD} \\
C_{\text{iss}} &= C_{GS} // C_{GD} \approx C_{GS} \\
C_{\text{oss}} &= C_{GD} // C_{DS}
\end{align*} \]
Relevant Parameters for Safe Gate Driving

2) Gate Voltage SOA

- $V_{gs+,max} = +25V$
- $V_{gs+,op} = +20V$
- $V_{gs-,op} = -5V$
- $V_{gs-,min} = -10V$
- $V_{gs+,op} = +22V$
- $V_{gs-,op} = -5V$
- $V_{gs-,min} = -10V$

- Wide negative range.
- Flexibility in design.
- Low risk of parasitic turn-on.
Contents

• Silicon Carbide at STMicroelectronics
• SiC MOSFET - Technology roadmap
• Gen 2 SiC MOS Technology
• STGAP2S Isolated Gate Driver
• Practical Example
✓ Up to 26 V supply voltage
✓ Miller CLAMP pin option
✓ Propagation delay < 100 ns
✓ CMTI > 100V/ns
✓ Galvanic isolation
  ✓ 1.7 kV in SO-8 package
  ✓ 6 kV in SO-8W package

STGAP2S
1700 V, 4A gate drivers

In Production
2019
STGAP2S CMTI test results @1500V

Test equipment
- DPO 7104C 1 GHz Oscilloscope
- IsoVu 1 GHz isolated differential probe
- 4 kV single-ended probe with GND clip
- DC linear power supply (+1500 V)

120 V/ns
GNDISO vs GND
GON-GOFF vs GNDISO

129 V/ns
STGAP2S

1700 V, 4A gate drivers

In Production

**Option 1:**
Single output and Miller CLAMP

**Option 2:**
Separated sink\source outputs

Recommended for SiC MOSFETs
Effectiveness of Active Miller Clamp

Tests in a Half-Bridge Inverter

Device Description

<table>
<thead>
<tr>
<th>Device</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>S1 &amp; S2</td>
<td>SCTW35N65G2V (55 mΩ, 650 V SiC MOS)</td>
</tr>
<tr>
<td>Gate Driver</td>
<td>STGAP2S, in both versions AMC and SO</td>
</tr>
</tbody>
</table>

Expected Waveforms in LS Switch
Assuming positive current

Circuit block diagram

Risk of Parasitic turn-on.
Operation outside SOA.

Dead-time
Active Miller Clamp

Legend of driver configuration
- **S-Out**: separated output
- **AMC**: Active Miller Clamp

Vgs-on=+18V
Vgs-off=-5V
Negative Deactivation Voltage

SCTW35N65G2V
70 mΩ, 650 V SiC MOSFET

Negative Glitch

Positive Glitch

Vgs [V]

Time [sec]
• Silicon Carbide at STMicroelectronics
• SiC MOSFET - Technology roadmap
• Gen 2 SiC MOS Technology
• STGAP2S Isolated Gate Driver
• Practical Example
## Application Example

### DC Chargers for Electrical Vehicles

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Value</th>
</tr>
</thead>
</table>
| Input voltage              | $V_{in}$ | 230V$_{ac}$ Ph-N  
|                            |        | 400V$_{ac}$ ph-ph                              |
| Max. Input Current         | $I_{in,max}$ | 32A/ph                                         |
| Max Power                  | $P_{in,max}$ | 7.36 kW/ph  
|                            |        | 22 kW total                                     |
| DC Link Voltage            | $V_{DC}$ | 400..1000Vdc                                    |
| Output Voltage             | $V_{out}$ | 200..500Vdc                                     |

<table>
<thead>
<tr>
<th>Configuration</th>
<th>Device</th>
<th>$R_{ds,on.typ}$ @ $T_{j}=25^°C$</th>
<th>Package</th>
<th>Number in parallel</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conf. 1</td>
<td>SCT50N120</td>
<td>52 mΩ @ $V_{gs}=20V$</td>
<td>HiP247</td>
<td>2x</td>
</tr>
<tr>
<td>Conf. 2</td>
<td>SCTW70N120G2V-4</td>
<td>25 mΩ @ $V_{gs}=18V$</td>
<td>TO-247-4 (Kelvin Source)</td>
<td>1x</td>
</tr>
</tbody>
</table>
## Comparison on Device Level

### Parameter Conditions

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>SCT50N120 (x2)</th>
<th>SCTW70N120G2V-4</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{ds,\text{on}}$</td>
<td>$V_{gs} = V_{g,\text{op}}$, $I_d = I_{d,\text{nom}}$, $T_j = 25^\circ C$</td>
<td>52 mΩ (26 mΩ)</td>
<td>25 mΩ</td>
</tr>
<tr>
<td>$R_{\text{th,j-c}}$</td>
<td>---</td>
<td>0.55 K/W (0.27 K/W)</td>
<td>0.45 K/W</td>
</tr>
<tr>
<td>$R_{\text{th,c-h}}$</td>
<td>---</td>
<td>~ 1 K/W (~0.5 K/W)</td>
<td>~ 1 K/W</td>
</tr>
</tbody>
</table>

**Dynamic Improvements must compensate thermal disadvantages of Conf. 2!**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>SCT50N120 (x2)</th>
<th>SCTW70N120G2V-4</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{\text{iss}}$</td>
<td>$V_{ds} = 800V$, $V_{gs}=0$, $f=1\text{MHz}$</td>
<td>1900 pF (3800 pF)</td>
<td>3500 pF</td>
</tr>
<tr>
<td>$C_{\text{oss}}$</td>
<td></td>
<td>170 pF (340 pF)</td>
<td>180 pF</td>
</tr>
<tr>
<td>$C_{\text{rss}}$</td>
<td></td>
<td>30 pF (60 pF)</td>
<td>30 pF</td>
</tr>
</tbody>
</table>
Experimental Results

Comparison Gen 1 vs. Gen 2 SiC MOS

Parameter Gain
- Amount of switch devices 50% less
- Heat-sink size 40% smaller
- PCB area 26% smaller
- Commutation loop size 43% smaller

Advantages on System Level

System Efficiency

\[ +2\% \]

\[ R_{g,\text{on}} = R_{g,\text{off}} = 3 \, \Omega \]

\[ \begin{align*}
\text{dV/dt during Commutation} \\
\text{Gen1} & \quad \text{Gen2} & \quad \text{Gen1} & \quad \text{Gen2} & \quad \text{Gen1} & \quad \text{Gen2} & \quad \text{Gen1} & \quad \text{Gen2} \\
\text{Turn-on} & \quad 38.4 \, V/\text{ns} & \quad 48.0 \, V/\text{ns} & \quad 27.0 \, V/\text{ns} & \quad 35.0 \, V/\text{ns} & \quad 39.7 \, V/\text{ns} & \quad 54.5 \, V/\text{ns} & \quad 28.8 \, V/\text{ns} & \quad 36.9 \, V/\text{ns} \\
\text{Turn-off} & \quad 50\% \text{ Power} & \quad 100\% \text{ Power} \\
\end{align*} \]
Based on planar structure, Gen 2 is a large improvement step in SiC MOSFET technology.

Product portfolio includes 650V and 1200V voltage classes, with very low $R_{ds,on}$ and innovative packages, like TO-247 4pin and D2PAK 7pin.

The combination of low Miller capacitance and extended negative gate voltage range enables fast and safe commutation.

Results in EV charger demonstrates the possibility to build up systems above 20 kW without the need of paralleling devices.
Wide bandgap transistors

From 650 V to 1700 V SiC MOSFETs featuring the industry’s highest temperature rating of 200 °C and a very small variation of the $R_{D\text{on,typ}}$ even at high temperatures.

Power MOSFETs

Broad range of breakdown voltages from -100 V to 1700 V, with low gate charge and low on-resistance, combined with state-of-the-art packaging.

IGBTs

Breakdown voltages from 300 to 1250 V. Low $V_{CE(sat)}$ for reduced conduction losses. Improved switch-off energy spread versus increasing temperature.

Power Bipolar

The range includes Darlington transistors and BJTs with a $V_{CE}$ from 15 to 1700 V.
Thank you!
Questions?