Designing with UnitedSiC FETs

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Manager Device Technology Development
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Contents

• Introduction to the UnitedSiC FET portfolio
• General Gate Drive Guidelines
• Using snubbers to manage switching waveforms
• Benefits of packages with Kelvin connections
• UnitedSiC FET User Guide
• Tips for paralleling TO packages
SiC Application Growth

Server & Datacenter

Lighting & Electronic Ballast

Electric Vehicles

Lab & Din Rail PSU

Battery Charging

Renewable Energy & Storage
UJ3C & UF3C Series, 650/1200V SiC FETs

Key Features
- Excellent body diode performance ($V_f < 2V$)
- Drive with any Si and/or SiC gate drive voltage
- High performance cascode configuration
- Superior thermal performance
- Integrated ESD and gate protection
- Kelvin package (UF3C Fast series)

Drop-in Functionality Without Changing Gate Drive Voltage
(Replaces Si IGBTs, Si FETs, SiC MOSFETs or Si Superjunction Devices)

12V/0V Operation Simplifies Upgrading

Superior Gate and ESD Protection

Innovative cascode configuration enables Si and SiC gate voltage compatibility

Integrated clamping diode protects gates from $25V$ and adds ESD protection
UnitedSiC Product Portfolio

- Schottky Diodes
- JFETs
- FETs

- UJ3C
  - Soft Switched
- UF3C
  - Hard Switched

- UnitedSiC Products
  - 3-Leaded packages
  - Source Kelvin Packages

- UnitedSiC Features:
  - Co-packaged high-performance Gen3 SiC JFETs with cascode-optimized MOSFET
  - Only standard gate drive SiC device in the market today
  - 650V and 1200V
  - Low on-resistance RDS(on)
  - Excellent reverse recovery
  - Low gate charge
  - Enhanced Thermal Performance
  - ESD protected, HBM class 2
  - Th (max op) = 175°C
UF3C performance benefits

<table>
<thead>
<tr>
<th>1200V Devices</th>
<th>UJ3C120040K3S</th>
<th>UF3C120040K3S</th>
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<td>Qrr (150°C)</td>
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<td>Rds(on)</td>
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<tr>
<td>VF(20A)</td>
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<tr>
<td>VF(20A)</td>
<td>1.3V</td>
<td>1.3V</td>
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</tbody>
</table>

- Lower losses for higher frequency switching circuits, especially where hard switching at turn-on is needed
- No changes to thermal resistance or current ratings
UF3C FAST SiC FETs in 4-lead kelvin connected package

All the benefits of UnitedSiC SiC FETs

PLUS

- Extremely fast switching
- Lowest switching losses
- Clean gate waveforms
- No false triggering
**Turn-off Waveforms**

- UF3C120040K3S: $E_{\text{off}} = 208 \mu J$
- UF3C120040K4S: $E_{\text{off}} = 170 \mu J$

**Turn-on Waveforms**

- UF3C120040K3S: $E_{\text{on}} = 1300 \mu J$, $\frac{di}{dt} = 3800\, \text{A/µs}$
- UF3C120040K4S: $E_{\text{on}} = 845 \mu J$, $\frac{di}{dt} = 7100\, \text{A/µs}$

800V, 40A, Half-bridge, RT, $R_{\text{gon}} = 3 \Omega$, $R_{\text{goff}} = 10 \Omega$, FWD: $V_{\text{gs}} = -5 \text{V}$, $R_{\text{g}} = 10 \Omega$; $R_{\text{SNUB}} = 10 \Omega$, $C_{\text{SNUB}} = 220 \text{pF}$
General Gate Drive Guidelines

- UnitedSiC cascode FET $V_{th}=5\text{V}$
- $V_{gs\text{max}} = +/-25\text{V}$
- Gate drive 0 to 12V is best, especially in ZVS applications
- No issues with negative gate drive. Any voltages +/-20V may be used with the right $R_g$ changes
- Devices are compatible with a wide range of gate drives and gate drive ICs – both Si MOS/IGBT drivers as well as newer SiC MOSFET drivers
- Also compatible with simple gate drive transformers
Gate charge comes from the LVMOS.

Same LVMOS used across many products leads to same Qg across many products.

Cascode dV/dt is controlled primarily by JFET built-in Rg (fixed) and secondarily by external MOSFET Rg (user controlled).

Generally, turn-off is much faster than turn-on in cascodes, so it needs a higher Rgoff.

**Figure 8** Typical gate charge

*at V_{DS} = 800V and I_D = 40A*
\( V_{GS} \) Effect on \( E_{SW} \) for TO247-3L

At higher currents, a \( V_{gs} > 12V \) allows faster turn-on for lower \( E_{on} \).

Not much difference below 15A
Comparison of Switching Losses with and without using Ferrite Bead

Ferrite bead

Part #: BLM41PG600SN1L
Description: FERRITE BEAD
60 OHM 1806 1LN

Looks like 100nH at 100MHz

- Ferrite beads may be used to control gate ringing.
- Smaller Rgoff values can be used with beads to reduce delay times, and reduce Eoff.

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<th>Customer Part Number</th>
<th>MURATA Part Number</th>
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<th>Rated Current (mA) (I)</th>
<th>DC Resistance (Ω) (Ω) max</th>
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<th>Values After Testing</th>
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<tr>
<td></td>
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<td>Typical at 85°C and 125°C</td>
<td>Typical at 85°C</td>
<td>Typical at 125°C</td>
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<td>0.04</td>
<td>For DC power line</td>
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- Operating Temperature: -55°C to +125°C
- Storage Temperature: -55°C to +125°C
Comparison of Switching Waveforms with and without using Ferrite Bead (Tj = 125°C, 800V-26A)

Ferrite beads not used:
- Switch $R_{gon}=1\Omega$, $R_{goff}=20\Omega$, $V_{gs}=-5$V to 15V
- FWD: $R_{goff}=20\Omega$, $V_{gs}=-5$V

Ferrite beads used:
- Switch $R_{g}=3.3\Omega$, $V_{gs}=-5$V to 15V
- FWD: $R_{g}=3.9\Omega$, $V_{gs}=-5$V

Using a ferrite bead, Turn-on peak current is lower with the bead since $di/dt$ is reduced. Since lower $R_g$ can be used with a ferrite bead, turn-off and turn-on delay times can be minimized.
Using Snubbers to manage switching waveforms

- UnitedSiC FETs have low $C_{OSS}$
- Snubber capacitances needed are 1 to 3X of $C_{OSS}$
- Therefore, very small snubber capacitances are needed to control voltage overshoot and reduce current ringing
- The net loss impact is 1-5% of $E_{ON} + E_{OFF}$
- Small surface mount components are usable, since Snubber $R_S$ loss is between 0.25W to 2W, depending on frequency (while switching 50A, 800V).
Snubber Design for UF3C120040K3S

- Cascode turn-off ringing may be reduced by high $R_{G,OFF}$ but this leads to long delay times.
- Waveforms in the second row show how the $V_{DS}$ and $V_{GS}$ ringing are dramatically improved with a small snubber, switching the FETs at 50A, 800V.
- Snubber loss is <2.5% of total $E_{ON} + E_{OFF}$ at 10A and < 1.5% at 50A.
Measuring snubber resistor loss

UF3C120040K4S HALF_BRIDGE

VDS 800V, ID 50A, 125°C, VGS 20V/-5V,
Rgon 50Ω, Rgoff 33Ω,
Snubber Cs 115pF, snubber Rs 10Ω

CH1: Snubber Rs voltage (20V/div);
CH2: Drain current (20A/div);
CH3: VGS (10V/div);
CH4: VDS (200V/div).

(a) Turn-off waveforms
(b) Snubber Rs voltage at turn-off CH1
(c) Turn-on waveforms
(d) Snubber Rs voltage at turn-on CH1
Snubber loss measured

UE3C120040K4S snubber Rs loss measurement vs. conventional $CV^2$ calculation.

This occurs because the $CV^2$ method assumes a constant charging voltage (infinite dV/dt), whereas practically, the device dV/dt regulates the maximum charging rate.
Benefits of Kelvin packages

- Switch faster by overcoming common source inductance
- Cleaner gate waveforms, even with much faster $di/dt$

DFN8X8  D2PAK-7L  TO247-4L
Reduced Turn-on losses ($E_{on}$)

Hard switched half-bridge

- Dramatic improvement in $E_{on}$ at higher current levels
- Snubber loss included
Reduced Turn-off losses ($E_{\text{off}}$)

Hard switched half-bridge

- Very low $E_{\text{off}}$ losses even at 50A
- Snubber loss included
Excellent choice in soft switched circuits too

Effective turn-off loss ≈

\[ E_{\text{off}}(\text{HS}) - (E_{\text{oss}} + E_{\text{cs}}) \]
# New SiC FET User Guide

## 650V FETs

- Device selector by spec
- RC snubber guide
- End application device selection

## Product Details

<table>
<thead>
<tr>
<th>Product Name</th>
<th>Package</th>
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<th>Gate Drive Voltage</th>
<th>Gate Drive Voltage</th>
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*Units: V, A, W, m, Ω, pF, uJ, mJ*
New SiC FET User Guide

1200V FETs

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### Product Name

<table>
<thead>
<tr>
<th>Package</th>
<th>Vdsmax</th>
<th>Id (25°C)</th>
<th>Id (100°C)</th>
<th>Ron (25°C)</th>
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### Gate Drive voltage

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### RC snubber guide

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### ZVS application

- Active rectifier, Totem Pole PFC, Full-bridge etc.
- LLC

### Hard switched applications

- Active rectifier, Totem Pole PFC, Full-bridge etc.

### Cs (pF)

<table>
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### Rs (Ω)

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*C0G* ceramic capacitors are most stable.

URL: https://unitedsic.com/cascodes/
Paralleling discrete devices for higher power

GENERAL GUIDELINES FOR PCB LAYOUT

- Symmetry
- Minimum PCB stray inductances
- Separate gate resistor
- Minimize capacitive coupling between gate and drain of each transistor.

Rds positive temperature coefficient aids current sharing

L_DS: main loop stray inductance
L_SS: common source inductance
Paralleling discrete devices for higher power

UnitedSiC FET paralleling is tolerant of typical parametric mismatches and temperature differentials

Vth mismatch

T_J mismatch of 40°C
Scalable SiC Cascode Power Blocks

Conventional Method:
Single external gate driver and capacitor at module level => All circuit legs switch through common parasitic inductance.

Preferred Method:
Local bus capacitance and gate drive buffer for each circuit leg => High frequency switching contained within each converter leg.

Power loop showing the Bottom of the PCB, the central "bus bar", and the gate drive loops on the Top layer.

Layout of 8 Parallel Legs
Scalable SiC Cascode Power Blocks

Power blocks have been built for half-bridges and TNPC units with up to 8X units in parallel.

Switching of a power block with 4X HS and 4X LS SiC FETs.
How the cascode FET works

JFET $V_{GS} = -MOSFET V_{DS}$

Cascode Internal Operation

- **Turn On**
  - MOSFET turns “On”
  - MOSFET $V_{GS} > MOSFET V_{TH}$
  - MOSFET $V_{DS} \sim 0$ V
  - JFET turns “On”
  - MOSFET $V_{DS} \sim 0$, JFET $V_{GS} \sim 0$ V
  - JFET $V_{TH}$ is $-6$ V typical

- **Turn Off**
  - MOSFET turns “Off”
  - MOSFET $V_{DS} < MOSFET V_{TH}$
  - MOSFET “Off”, $V_{DS}$ rises $> 6$ V
  - JFET turns “Off”
  - High Voltage Across JFET $V_{DS}$
Easy to Cascode JFET Design

- UnitedSiC JFET has zero drain-source capacitance
- No drain-source-gate voltage divider
- Good for ZVS operation
- Stable

Body Diode $V_F$: UnitedSiC FET vs SiC MOSFET

**Typical UnitedSiC FET**

- Low $V_F$ & $Q_{rr}$ eliminates need for separate anti-parallel diode

**Typical SiC MOSFET**

Figure 10 3rd quadrant characteristics at $T_J = 25^\circ C$

Figure 14. 3rd Quadrant Characteristic at 25 $^\circ$C
What controls switching speeds

- Turn-on $di/dt$ can be slowed by MOSFET $R_{gon}$ in a TO247-3L, where $L_s$ de-biases the $V_{gs(MOS)}$. So higher $V_{gs}$ values can speed up $di/dt$.
- The upper limit to the $di/dt$ is set by the fact that the JFET $V_{th}$ is fixed, and the JFET experiences a $V_{GS(JFET)}=-V_{DS(MOS)}$ that is fixed. The internal inductance and the $R_{GJFET}*(C_{gsJ}+C_{oss(MOS)})$ sets this maximum $di/dt$.
- Once the MOSFET has turned off enough to pinch-off the JFET, $dV/dt$ is largely regulated by the $C_{gdJ}*R_{GJFET}$. However, slowing the MOSFET drain node using an external $R_{goff}$ can influence the turn-off rate, essentially slowing the gate voltage applied to the JFET at turn-off.
Measured Turn-on Energy Loss, $\text{di/dt}$ and $\text{dv/dt}$ with 600V Inductive Load. FWD: UJC1206K
Measured Turn-off Energy Loss, di/dt and dv/dt with 600V Inductive Load Condition. FWD: UJC1206K
Comparing G2, G3 cascodes and SiC MOSFETs in half-bridge

**UJC1210K, 12V/-5V**
- $R_{on} = 2.3$ Ω, $R_{off} = 10$ Ω, $E_{on} = 406$ uJ
- $\frac{di}{dt} = 1.28$ A/ns, $\frac{dv}{dt} = 69$ V/ns

**UJ3C120080K3S, 15V/-5V**
- $R_{on} = 1$ Ω, $R_{off} = 20$ Ω, $E_{on} = 392$ uJ
- $\frac{di}{dt} = 2.78$ A/ns, $\frac{dv}{dt} = 78$ V/ns

**C2M080120D, 18V/-5V**
- $R_{on} = 6$ Ω, $R_{off} = 5$ Ω, $E_{on} = 446$ uJ
- $\frac{di}{dt} = 2.1$ A/ns, $\frac{dv}{dt} = 71$ V/ns

**UJC1210K**
- $R_{on} = 2.3$ Ω, $R_{off} = 10$ Ω, $E_{on} = 101$ uJ
- $\frac{di}{dt} = 4.2$ A/ns, $\frac{dv}{dt} = 86$ V/ns

**UJ3C120080K3S**
- $R_{on} = 1$ Ω, $R_{off} = 20$ Ω, $E_{on} = 107$ uJ
- $\frac{di}{dt} = 3.7$ A/ns, $\frac{dv}{dt} = 85$ V/ns

**C2M080120D**
- $R_{on} = 5$ Ω, $R_{off} = 5$ Ω, $E_{on} = 116$ uJ
- $\frac{di}{dt} = 2.3$ A/ns, $\frac{dv}{dt} = 60$ V/ns
UJ3C120080K3S Half-bridge Vgs drive +15V/-5V
Rgon=1ohm, Rgoff=20ohm, 125C

Eon = 217 \mu J
Eoff = 30 \mu J

Eon = 268 \mu J
Eoff = 45 \mu J

Eon = 328 \mu J
Eoff = 68 \mu J

Eon = 392 \mu J
Eoff = 107 \mu J

Eon = 559 \mu J
Eoff = 167 \mu J
UJ3C120080K3S Half-bridge Vgs drive +15V/-5V
Rgon=2.3ohm, Rgoff=8ohm, 125C

Eon = 236 uJ
Eoff = 29 uJ

Eon = 347 uJ
Eoff = 69 uJ

Eon = 440 uJ
Eoff = 94 uJ

Eon = 625 uJ
Eoff = 134 uJ
UJ3C switching characteristics
80m, 1200V

Figure 18 Clamped inductive switching energy vs. drain current at $T_J = 150^\circ$C

Figure 20 Clamped inductive switching turn-off energy vs. $R_{G,EXT_{OFF}}$

Figure 21 Clamped inductive switching energy vs. junction temperature at $I_D = 20A$
UJ3C switching characteristics
30m, 650V

Figure 18 Clamped inductive switching energy vs. drain current at $T_J = 150°C$

Figure 20 Clamped inductive switching turn-off energy vs. $R_{G,EXT\_OFF}$

Figure 21 Clamped inductive switching energy vs. junction temperature at $I_D = 50A$
Measured Qrr of UJ3C120040K3S vs UF3C120040K4S

Minimum Qrr in a cascode is Qc, the integrated Coss charge.
UF3C120080K4S
Half-Bridge Switching Energies

Inductive load: 800V
Tj = 25°C
Rg_on = 8.5Ω
Rg_off = 20Ω

Switching Energy (μJ)

Eon

Eoff

Tj (°C)

Switching Energy (μJ)

Eon

Eoff

Load Current, I₀ (A)
UF3C120080K4S Switching Waveforms
800V, Tj = 25°C, Vgs = -5V/+12V

Rg_on = 1Ω
Rg_off = 47Ω
Turn-on di/dt = 8563A/us

Rg_on = 21Ω
Rg_off = 47Ω
Turn-on di/dt = 1995A/us
Since turn-on is no longer critical, it should generally be possible to use a single \( R_{goff} \).

Depending on current, 5-20 ohm works well.

Sufficient to limit gate drive to 0-12V – no benefit with higher \( V_{gs} \), no benefit with negative gate drive.

A bead can still be used if currents are high, or if a low \( R_{goff} \) is required to minimize delay time at high frequencies.
650V cascode – Totem Pole PFC

Uniquely qualified for use in CCM Totem Pole PFC due to excellent Body Diode

Freewheeling current

Bridgeless Totem-Pole PFC
85 – 265 VAC in, 400 VDC out, 100 kHz

Efficiency vs. Output Power (W)

UnitedSiC
Snubber Design for UF3C120080K4S series

Test Conditions

- Top switch is the freewheeling device
- VDS, ID are measured for the bottom switch
- VGS: +15V turn on, -5V turn off
- Rgon 10Ω, Rgoff 10Ω
- VDS 800V
- ID: 25A
- Temperature: 120°C both top & bottom switch
- Snubber: 10Ω, 220pF
- When adding a snubber, switching loss includes both device and snubber loss.
- DUT: UF3C120080K4S
Snubber Design for UF3C120080K4S series

- The measurement on the left shows more VDS ringing at turn-off transient than turn-on.
- Therefore the snubber should be placed on the bottom switch.
Snubber Design for UF3C120080K4S series

Guideline for snubber design

The VDS ringing frequency is 100MHz (f0). Adding a Cadd (220pF) reduces frequency to 42MHz (f1). Therefore the circuit stray capacitance CLK is 47.1pF.

\[
CLK = \frac{C_{add}}{(f_0/f_1)^2 - 1}
\]

Therefore the circuit leakage inductance LLK is 54nH.

\[
LLK = \frac{1}{(2\pi f_0)^2 \cdot CLK}
\]

If damping factor \(\zeta = 1.6\), \(Rs = 10\Omega\)

\[
Rs = \frac{1}{2\zeta} \sqrt{\frac{LLK}{CLK}}
\]

If cutoff frequency \(fc = 68.5\text{MHz}\), \(Cs = 220\text{pF}\).

\[
Cs = \frac{1}{2\pi Rs fc}
\]
Snubber Design for UF3C120080K4S series

Trade off’s using a snubber

No Snubber
Eon = 363uJ, Eoff = 64uJ

With Snubber
Eon* = 371uJ, Eoff* = 147uJ

- Cascode turn-off ringing may be reduced by high Rgoff but this leads to long delay times
- Quick and easy solution to use fast SiC devices in existing designs without causing excessive ringing

The Eon*, Eoff* with snubber are the total loss of device and snubber.
Customer Reference: Micropower

- Phase shifted Full bridge
  - Need for an excellent body diode
- 10kW battery charger
- Technological partnership
- RESULTS:
  - 30% higher output power with UnitedSiC FET in same dimensions
  - Easy to replace Si-FET replacement using standard gate drive
  - 1.5% higher efficiency
UnitedSiC FET advantage in PSFB

- Previous technologies include IGBT, super-junction MOSFET, and SiC MOSFET
- IGBTs have very high turn-off switching power loss, slow-switching reverse diode
- Super-junction MOSFETs have larger chip size, slow-switching reverse diode
- SiC MOSFET has larger chip size, asymmetric gate drive (-5 to 18 V typically)
- UnitedSiC FET is the best performing PSFB switch
Battery Charger topology

A non controlled traditional battery charger (rectifier) provides a simple direct AC/DC conversion

Disadvantages of this solution are:
- Low efficiency
- Large physical size
- Long charge times
- Charge depends on changes in the mains supply (with overcharge danger in the final charge phase)

In modern battery chargers these disadvantages are solved with an indirect AC/DC conversion, by passing through an intermediate DC/DC conversion.

The main advantages of this solution are:
- High efficiency
- Reduced dimensions
- Short charge times
- Charge independent from the changes of the mains supply
- Electronic control that provides the desired charge curve