100V ENHANCEMENT MODE HIGH ELECTRON MOBILITY TRANSISTOR (HEMT)

Michele Rossitto

Marketing Director
MOSFETs and Power ICs
100V GaN in PowerPAK® 6 x 5 mm² Package

Enhancement Mode GaN Transistor

Superior 
\[ R_{DS} \cdot Q_g \] FOM

Re-workability

Industry Low \( Q_g \)
\( Q_g \) of 8 nC

Built-in ESD

Protective encapsulation

Classic PowerPAK® Construction

Ultra Low 
\( Q_{oss} / E_{oss} \)
21 nC and 0.4 \( \mu J \)

6 m\( \Omega \)

Clip bonding

Leadership \( Coss \)
For power supplies in telecom and servers

FOM = 48 m\( \Omega \)-nC
Vishay 100V eGaN Highlights

- eMode Gan in industry standard 6 x 5 mm² PowerPAK®
  - Drop in replacement for existing Si package with minimal PCB modification. No special solder profile needed. Easy to inspect

- Clip bonded drain and source terminals resulting in low package impedances.

- Vishay proprietary ESD protection for the sensitive gate
  - Kelvin source connection for clean gate drives

- 3rd quadrant conduction without body diode
  - Zero $Q_{rr}$ in synchronous modes of operation

- Low $C_{oss}$ related losses. $Q_{oss}$ / $E_{oss}$ are 21 nC / 0.4 uJ
  - Efficient operation at higher switching frequencies

- Low $Q_g$ of 8 nC. $Q_{gs}$ of 1 nC and near-zero $Q_{gd}$
  - Gate switching times of 10-12 nsec even with modest gate drive
  - Drastically reduces dead time and related 3rd quadrant losses.
100V GaN in PowerPAK® 6x5 mm² Package

Excellent $R_{DS-Qg}$ FOM Increases Efficiency
- Enhancement mode device
- $R_{DS-Qg}$ FOM = 48 mΩ·nC
- 6 mΩ
- Clip construction allows high current handling

Target Applications
- DC/DC converters
- Power supplies for mission critical applications
- Solar micro inverter
- Motor drive control

Optimized for Switching Applications
- Kelvin source connection reduces gate loop inductance to minimize ringing
- Industry low $Q_g$ and $C_{oss}$
- Minimized $Q_{rr}$ prevents ringing

Package Is Optimized for PCB Surface Mounting
- Encapsulated package is easier for rework
- Package dimension is identical to PowerPAK® SO-8

Sampling in 2019

<table>
<thead>
<tr>
<th>Parameters</th>
<th>SiR04G10D</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Package Dimension (mm x mm x mm)</td>
<td>6 x 5 x 1</td>
<td>mm x mm x mm</td>
</tr>
<tr>
<td>$V_{DS}$</td>
<td>100</td>
<td>V</td>
</tr>
<tr>
<td>$R_{DS(ON)} @ V_{GS} = 6V$</td>
<td>6</td>
<td>mΩ</td>
</tr>
<tr>
<td>$Q_g$</td>
<td>8</td>
<td>nC</td>
</tr>
<tr>
<td>$Q_{gs}$</td>
<td>0.3</td>
<td></td>
</tr>
<tr>
<td>$Q_{gd}$</td>
<td>0.01</td>
<td></td>
</tr>
<tr>
<td>$C_{oss}$</td>
<td>275</td>
<td>pF</td>
</tr>
<tr>
<td>$R_{DS-Qg}$ FOM</td>
<td>48</td>
<td>mΩ·nC</td>
</tr>
</tbody>
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Top $R_{DS-Qg}$ FOM

- Optimized for switching applications

Competitive $R_{DS(ON)}$

- Reduces conduction loss
- 6 mΩ at $V_{GS} = 5V$

16% lower $R_{DS-Coss}$ FOM

- Reduces loss from charging and discharging $Q_{oss}$ during ZVS intervals

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Vishay 100V GaN vs. Competitors

<table>
<thead>
<tr>
<th></th>
<th>Vishay 100V GaN</th>
<th>Competitor 1</th>
<th>Competitor 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{DS-Qg}$ FOM (mΩ-nC)</td>
<td>90.0</td>
<td>80.0</td>
<td>70.0</td>
</tr>
<tr>
<td>Typical $R_{DS(ON)}$ (mΩ)</td>
<td>8.0</td>
<td>7.0</td>
<td>6.0</td>
</tr>
<tr>
<td>$R_{DS-Coss}$ FOM (mΩ-pF)</td>
<td>3500</td>
<td>3000</td>
<td>2500</td>
</tr>
</tbody>
</table>
Technology Roadmap for 100V Products

**Roadmap of Silicon**

Conventional solutions with aggressive improvement; targeting mass market

- **SiR668ADP**
  - FOM = 216 mΩ-nC
  - Typ. $R_{DS(ON)}$ = 4 mΩ
  - $Q_g$ = 54 nC
  - 20% improvement on $Q_g$ of 250M cell SG

- **SiR668DP**
  - FOM = 288 mΩ-nC
  - Typ. $R_{DS(ON)}$ = 4 mΩ
  - $Q_g$ = 72 nC
  - Aims for leadership $R_{DS}$-$Q_g$ FOM with low $Q_{oss}$

**Roadmap of Wide Band Gap**

Revolutionary FOM for mission critical designs without concern of budget

- **100V e-GaN**
  - PowerPAK 6 X 5
  - SiR04G10D
  - FOM = 48 mΩ-nC
  - Typ. $R_{DS(ON)}$ = 6 mΩ
  - $Q_g$ = 8 nC

FOM = 125 mΩ-nC

PowerPAK SO8

- Typ. $R_{DS(ON)}$ = 3.4 mΩ
- $Q_g$ = 35 nC
- Aims for leadership $R_{DS}$-$Q_g$ FOM with low $Q_{oss}$
100V GaN benchmarked against best-in-class 100V silicon in a 48V $\rightarrow$ 12V synchronous buck converter.

Both devices tested till they reached $T_j \sim 100$ °C

- **GaN tested to 500 kHz.**
- **Silicon limited to 250 kHz.**
GaN vs Si – Synchronous Buck Efficiency

- Even at 2x switching frequency GaN is more efficient
- Efficiency difference is more pronounced at light load
  - Silicon has constant 4W power loss, arising from Qrr related losses
- Benefits of zero Qrr can be significant for high voltage synchronous buck and SSR applications.
$V_{gsH}$ and $V_{gsL}$ Comparison

- Drawn to different time scales – 100 ns/div for GaN and 200 ns/div for Si
- Waveforms depict high side and low side gate voltages on no load and without any voltage on the DC bus
  - Dead time set to 20 ns for both

- GaN has no crossover issues @ 20 ns. Low Qg can handle very short transition times for gate rise and fall.
  - Reduces dead time requirements and body diode conduction loss
- With Si, 20 nsec dead time results in crossover of gate voltage and shoot through.
Si switches slowly and has shoot through under different conditions.

All waveforms with common 20 nsec deadtime
GaN vs Si – Qrr Matters

- In a synchronous buck LS MOSFET always conducts in 3\textsuperscript{rd} quadrant
- Turning OFF the LS is not an issue with GaN which has no body diode
  - HS GaN can turn ON under 20 nsec without shoot through
  - No diode reverse recovery time
    - … or losses!

- With silicon, body diode of the LS MOSFET must be hard commutated
  - Reverse recovery time always gets added to the dead time
  - Shoot through conditions exist as the HS MOSFET turns on
  - Increased losses prevent higher frequency operation with silicon
THANK YOU!