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- Controllers & Processors
- Internet-of-Things

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### Best in Class: In Stock for Immediate Shipment?*

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*AspenCore’s 11th Design Engineer and Supplier Interface Study gathered information from engineers regarding their need for product information and other services, as well as how and when they interface with suppliers and how they see the quality and value of that interface. 1,764 U.S. engineers participated in this year’s web-based survey. The results represent those surveys completed by April 2016. When asked “Best in Class: Parts in stock for immediate delivery?” The chart above shows the results among the industry’s electronic component distributors.

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Dear Readers,

It is commonplace that not only the embedded industry is subject to continuous change but the whole life itself. But the change in the embedded industry took place very fast. Let’s have a look back in history! Do you remember the first computers in the 1970s? Huge rack systems with only a little computing power compared to mobile handsets nowadays. In the 1980s and 1990s the advent of the Personal Computer took place and these PCs became portable due to the ongoing miniaturisation manifested in Moore’s Law. But all these computer systems were more or less stand-alone because computer networks were used only in very special applications but not in general and the Internet was only in its beginning for universal use. Around the year 2000 the increased general application of the Internet and the Smartphones started. This meant that the embedded industry needed server computing power on one hand and also high performance computing power for the mobile Smartphones. The merger of IT and embedded technologies began. And in any of these stages of development different computing devices were needed - microprocessors and -controllers, DSPs, computer architectures, housings, and entire embedded systems – just to name a few.

And the development is going on. Today the Internet starts to free itself from human interaction and work independently. This again requires of course new computing devices to succeed in the new area of the Internet of Things. An area in which anonymous Cloud computers and fog servers as well as various networking technologies the plethora of “things” interconnect and enable the data exchange between all of these devices. This issue proves that the future has just begun. Our cover story starting at page 6 introduces highly dense motherboard series with integrated system on a chip which provide scale and flexibility across low power and high performance for the edge. It enables the suited computational workloads for data analysis that span across storage, communication, and security systems. An interesting inside in the future of next generation COMs gives the interview starting at page 10. It also shows that standard bodies are still playing a major roll in this future.

Will IoT create a beautiful new world in general? There are some important preconditions to ensure the safe and secure operation of the IoT. It is clear that the interconnected components whether they are small devices like Smartphones or huge industrial plants have to work 24/7 without any interruption. Many hard and software companies work hard to ensure this safe operation. But I believe more important is security because due to the fact that many of the IoT connections are wireless they are prone to unauthorized access. Also in security many companies are involved to reach the goal of a secure IoT. But it shows also that not a single company can solve the problems – there must be cooperation between players in the embedded industry. We are just at the beginning of this new area and future must tell whether IoT will be more curse or blessing. Let’s hope blessing will prevail.

Yours Sincerely

Wolfgang Patelay
Editor
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### High Performance SoC Motherboards for Responsive Computing

This article introduces a highly dense motherboard series with SoC (System on Chip) which provide scale and flexibility across low power and high performance solutions for the edge. It enables the suited computational workloads for data analysis that span across storage, communications and security systems.

### The future starts now: Next generation Computer-on-Modules

With the release of two new specifications from the standardization bodies PICMG and SGET, there are significant improvements happening right now to simplify the design of next generation carrier-grade network equipment, cloud services based on embedded edge and fog servers as well as IoT devices. Boards & Solutions spoke with Dirk Finstel, Executive Vice President Global Module Computer Product Segment with ADLINK, to get the latest insights from one of the originators of these standards.

### Graphics power for high-volume digital signage installations

This article highlights the cooperation of semiconductor, computer module and display companies to create powerful digital signage systems at affordable cost.

### IoT opportunity demands new approach to MCU-based embedded designs

The stakes in the IoT market are high. In this hyper-competitive environment, traditional approaches to product development hardly suffice. This article introduces the Renesas Synergy Platform, each element of which, silicon, software, tool ecosystem, kits and reference designs, contributes to a shorter, quicker development cycle.

### Processors with multiple industrial communication protocols on chip

This article introduces the Sitara processors which are tailored for industrial automation and help to form a complete industrial automation platform.

### LoRA wireless networking standard opens up the smart city

This article describes the advantages of the long range LoRa network for creating IoT applications, not only in cities but also spreading into the rural environment.
SECURING THE INTERNET OF THINGS

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High Performance SoC Motherboards for Responsive Computing

By Kanti Bhabuthmal, Supermicro

This article introduces a highly dense motherboard series with SoC (System on Chip) which provide scale and flexibility across low power and high performance solutions for the edge. It enables the suited computational workloads for data analysis that span across storage, communications and security systems.

With exponential growth and innovation in the worldwide IoT (Internet of Things) industry, millions of smart edge devices are being added every second. As a result, there is an enormous growth in data generation, data analytics and data storage requirements. There is also a need to provide scalable and flexible solutions to move, manage, analyze and store this data at the edge with minimum tolerance for latency. In most use cases, data needs to be processed at the edge and response times cannot suffer due to latency delays from multiple hops to and from data centers. Latency is non-tolerant in many instances and backhaul can impact both performance and cost of moving data back and forth from the data center. In most use cases real-time data analysis at the edge is important, while streaming and batch processing of historical data for in-depth analysis is more ideal in the cloud. Massive amounts of historical data still need to be parsed and analyzed. This can be done at the cloud including storing and archiving large data sets for future reference.

There are a few advantages of managing data computation and decisions making at the edge. The first are maximizing productivity by managing industrial equipment and machinery and optimizing efficiencies by minimizing fuel consumption in the transportation industry. Managing extreme conditions in a chemical industrial plant and managing inventory in a retail or grocery store chain as well as managing logistics for the last mile delivery of packages with routing algorithms based on package addresses, concentration and traffic conditions are other advantages. Managing digital signage with real-time data in public venues and large gatherings in Smart Cities with digital surveillance for managing traffic, parking and crime prevention complete the advantages.

With the enormous growth of (IoT) data connected devices in mobile networks, carriers require a fully converged and scalable high-performance solution at the edge. Supermicro SoC solutions are helping IoT platform providers address these edge convergence needs by introducing a converged yet scalable building block solution with the new Supermicro X10SDV family of embedded/server motherboard designs. New sets of products based on Intel® Xeon® processor D SoC offer converged yet scalable solutions that can efficiently manage workloads at the edge. This enables data to be securely managed, moved, analyzed and stored at the edge and in the cloud. Designed expressly for consolidating infrastructure at the intelligent edge, these optimized solutions offer exciting possibilities when paired with the latest Intel® Xeon® processor D product family. The combination brings new performance, density, low power consumption, and cost savings to a variety of compute, storage and networking workloads.

Analyzing and processing of data by collecting, inspecting and using data models with the goal of decision making and discovering useful information. SoC solutions at the edge provide the ability to quickly analyze data in real time and provide intelligent feedback to smart sensors locally to what is relevant. Cryptographic systems are used for encryption and decryption and to secure data for transport and access authentication. SoC solutions can act as edge managers for associating user rights and restrictions with the established identity by identity management and creating security certificates. The systems can regulate access to edge resources based on the roles of individual users. In this context, access of an individual user can be restricted to perform a specific task, such as view, create, or modify a file. These SoC solutions can offer data and traffic management across multiple networks with connectivity management or via secure transport using Tunnel/VPN applications.

Dynamic data or transactional data are situated where information is constantly being collected and can be stored locally for quick access. Persistent data can be backhauled to
COM Express® Type 7

Bringing 16-core Server Grade Intel® Xeon® Processor D Family SoC and 10GbE to COM Express®

COM Express Basic Size Type 7 Module

Express-BD7

- 32GB dual channel DDR4 up to 2400 MHz
- 2x 10GbE, 1x GbE and NC-SI
- Intel® TXT supported
- TDP 45W
- 2x SATA 6 Gb/s, 4x USB 3.0/2.0, 24 PCIe lanes (6 controller)
- Extreme Rugged operating temp.: -40°C to +85°C (opt. with selected SKUs)
cloud for batch processing or archiving. SoC solutions provide options for cold, warm or hot storage that scale with performance and capacity with different cost points, including M.2 (PCI-e 3.0) storage expansion slots.

Network connectivity provides the ability to transport small data packets from multiple smart devices to edge devices and large to medium to large packets between edge devices and large payloads to the cloud. These SoC solutions can operate as single entities or as fabrics to avoid a single point of failure. SoC solutions provide a choice of LAN connectivity ports with 1G/10G Ethernet speeds, along with mini-PCIe expansion port for Wi-Fi, ZigBee, and 3G wireless connectivity options. IoT platform and solutions providers can unify hardware requirements that are scalable with SoC solutions and to address specific vertical market segments.

X10SDVSoC family with its server-class capabilities offers the industry the most converged infrastructure and a low total cost of ownership (TCO) to a wide range of embedded applications. The motherboard is a small mini-ITX or Flex-ATX form factor solution providing up to 22 storage devices (16x6Gbs SATA3/SAS2 ports, 6x SATA3 ports), 8 LAN ports (including Dual 10GbE fiber connectivity), and IPMI for remote management. The solution is optimized for 1U and 2U rack environment, including a new 1U solution for 12x3.5” hot-swap drives and 2U solutions for 24x 2.5” hot-swap drives. Features include redundant high-efficiency power supplies, specially designed optimized cooling, and dual PCI-e 3.0, Mini PCI-e/mSATA and M.2 expansion slots for superior network and additional storage options.

Powered by the latest Intel® Xeon® processor D product family with up to 16 cores, the high-density hyper-scale X10SDV family provides scalable power and performance solutions. Based on Intel 14nm process technology these processors couple lower power consumption with the performance of up to 16 cores. The processor family enables new options for infrastructure optimization, bringing the performance and advanced intelligence of Intel® Xeon® processors into dense, lower-power SoCs.

These powerful SoCs include improved cache sizes and support up to 128GB DDR4 ECC registered memory. Other advanced processor features include Intel Virtualization Technology, Intel® Hyper-Threading Technology, Intel® Hyper-Threading Technology, Intel® Advanced Vector Extensions 2 (Intel AVX2); Intel QuickData Technology, providing up to 22 storage devices (16x6Gbs SATA3/SAS2 ports, 6x SATA3 ports), 8 LAN ports (including Dual 10GbE fiber connectivity), and IPMI for remote management. The solution is optimized for 1U and 2U rack environment, including a new 1U solution for 12x3.5” hot-swap drives and 2U solutions for 24x 2.5” hot-swap drives. Features include redundant high-efficiency power supplies, specially designed optimized cooling, and dual PCI-e 3.0, Mini PCI-e/mSATA and M.2 expansion slots for superior network and additional storage options.

MEN becomes member of UNIFE
Recently MEN Mikro Elektronik has become a member of UNIFE. As an expert for safe and reliable electronics on rolling stock and wayside, MEN will actively contribute to the digitalization of the rail market and the development of European standards.

News ID 4430

congatec: highly flexible IoT gateway system
congatec introduces its flexible IoT gateway solution, which is application ready and easily customizable for rapid field deployment. The congatec IoT gateway offers extreme levels of flexibility in terms of processing performance and software integration, able to host up to 8 wireless antennas that can be connected to 3 mini PCI Express slots and 6 internal USB based slots for wireless and wired connectivity modules. Customized system designs are also available upon request.

News ID 4432

DFI: fanless Embedded computer features Quad Core Atom E3800 processor
DFI Tech now offers a higher performance quad core processor in its rugged EC series fanless computing systems. The EC700-BT Fanless Embedded System from DFI Tech features an Intel Atom E3845 quad core 1.91GHz processor and 4GB of DDR3L ECC on-board memory. The lightweight fanless system is rugged, conforming to MIL-STD-810F (514-SC-2) for vibration and can handle 15G half sine wave of shock for 11 ms in 3 axes.

News ID 4430

Artesyn to demonstrate ControlSafe Platform at InnoTrans
Designed to deliver best-in-class platform hardware availability of six nines (99.9999%), Artesyn’s ControlSafe Platform is designed to meet the functional safety, reliability and availability requirements mandated by rail standards and specifications. This makes Artesyn’s ControlSafe Platform ideal for deployment in safety application environments to protect investment in rail infrastructure.

News ID 4429
Supermicro Product Highlights

- The E300-8D is a small Mini-1U form factor system solution built with Intel® Xeon® processor D-1518 (4-core, 35W) SoC. Supports up to 128GB DDR4 ECC RDIMM, 2.5” drive bay or PCI-E 3.0 x8 AOC, Mini PCI-E (mSATA), M.2 PCI-E 3.0 x4, 2x USB 3.0, 2x 10G SFP+, 6xGbE and a dedicated IPMI LAN port.

- The SYS-5018D-FN4T is a small 1U short-depth rack mount front I/O server solution built with Intel® Xeon® processor D-1541 (8-core, 45W) SoC. Supports 2x 3.5” or 4x 2.5” drive bays, up to 128GB DDR4 ECC RDIMM, PCI-E 3.0 x16 AOC, M.2 PCI-E 3.0 x4, TFM 2.0 header, 2x 10GBase-T and 2xGbE and a dedicated IPMI LAN port.

- The X10SDV-TP8F is a small Flex-ATX form factor solution built with Intel® Xeon® processor D-1518 (4-core, 35W) SoC. Supports up to 128GB DDR4 ECC RDIMM, 2x PCI-E 3.0 x8 slot, M.2 PCI-e 3.0 x4, Mini PCI-E 2.0, 4x SATA3 (6Gbps) ports; RSTe, TPM 2.0 header, 2 10G SFP+ and 6x1GbE and a dedicated IPMI LAN port.

- The X10SDV-TLN4F is a small Mini-ITX form factor solution built with Intel® Xeon® processor D-1541 (8-core, 45W) SoC. Supports up to 128GB DDR4 ECC RDIMM, PCI-E 3.0 x16 slot, M.2 PCI-E 3.0 x4, 6x SATA3 (6Gbps) ports; RSTe, TPM 2.0 header, 2x 10G and 2xGbE and a dedicated IPMI LAN port.

- The X10SDV-7TP8F is a small Flex-ATX form factor solution built with Intel® Xeon® processor D-1587 (16-core, 65W) SoC. Supports up to 128GB DDR4 ECC RDIMM, 2 PCI-E 3.0 x8 slots, M.2 PCI-E 3.0 x4, Mini PCI-E 2.0 (mSATA), 4x SATA3 (6Gbps) ports; RSTe, 16x SATA3 (6Gbps) ports; LSI 2116, TPM 2.0 header, 2x 10G SFP+ and 6xGbE and dedicated IPMI LAN port.

- The SYS-5018D-4-AR12L is optimized for 1U environment built with Intel® Xeon® processor D-1518 (4-core, 25W) with 12x 3.5” hot-swap SAS2/SATA3 drive bays, 2x 10G SFP+ and 2x GbE LAN. The solution features redundant high efficiency power supplies, optimized cooling design, expansion slots for flexible networking options.

- The SYS-E200-8D is a small Mini-1U form factor system solution built with Intel® Xeon® processor D-1528 (6-core, 35W) SoC. Supports 2.5” drive bay, up to 128GB DDR4 ECC RDIMM, M.2 PCI-E 3.0 x4, 2x USB 3.0, 2x 10G, 2x GbE and a dedicated IPMI LAN port.
The future starts now: Next generation Computer-on-Modules

Interview with Dirk Finstel, ADLINK Technology

With the release of two new specifications from the standardization bodies PICMG and SGET, there are significant improvements happening right now to simplify the design of next generation carrier-grade network equipment, cloud services based on embedded edge and fog servers as well as IoT devices. Boards & Solutions spoke with Dirk Finstel, Executive Vice President Global Module Computer Product Segment with ADLINK, to get the latest insights from one of the originators of these standards.

B&S: ADLINK Technology is one of the leading embedded Computer-on-Module vendors in the world and has significantly shaped recently released new SGET SMARC 2.0 specification and pre-release of the new COM Express Type 7 specification by PICMG. What is the reason behind the concurrent launch of two new next generation standards?

Finstel: The tremendous performance improvements within carrier networks together with the trends to IoT, cloud computing and network virtualization change the way we want to set up new applications. That makes it necessary to specify Computer-on-Module standards that meet these new requirements most efficiently.

B&S: Aren’t Computer-on-Modules one-for-all platforms and therefore suitable for nearly all embedded system designs? Why do we need new standards?

Finstel: Yes. They are of course standardized, application-ready computing cores for customized designs with carrier boards and thus universally applicable. But the standards are only defined for their specific application areas. The well-established COM Express Type 6 specification, for example, is designed to meet the requirements of powerful stand-alone rugged systems that, from a performance, graphics and TDP point of view, are comparable to what we use on the desktop PC and notebook level. But with the IoT and cloud trends we need high-end cloud computing intelligence and optimized I/Os for headless edge and fog server technologies, and that’s what COM Express Type 7 as well as the latest Intel Xeon processors with a maximum power draw of 65 watts are designed for. And we need IoT gateways and a large number of cloud-connected smart devices in the field that support smart cameras and wireless antennas natively in order to build, for example, smarter and more secure cities or to connect vending machines and ticketing systems with their dedicated clouds. These are major application areas that SMARC 2.0 is designed for.

B&S: So you see SMARC 2.0 as the platform for IoT connected devices and IoT gateways; and COM Express Type 7 modules for headless edge and fog servers as well as virtualized carrier-grade network equipment?

Finstel: Yes. These are among the most important new horizontal application areas for which nearly every vertical market that uses embedded computing technologies needs to be prepared.

B&S: Let’s start going more into the details. What are the differences between COM Express Type 7 and the widely accepted COM Express Type 6 specification?

Finstel: One of the most fundamental innovations of the COM Express Type 7 pin out is the support of more performance and more I/O bandwidth with server-grade headless Intel Xeon processors that have a maximum power draw of 65 watt, up to four 10GbE KR interfaces and up to 32 PCIe lanes. On the module, they are implemented as 10GbE single backplane lanes according to IEEE 802.3, paragraph 49. The physical shaping of the 10GbE interfaces takes place on the carrier board itself. Here, developers can define the signal transmission as optical SFP+, copper cable (T) or as KR – in order to implement, for example, module-to-module connections on multi-module carrier boards. This provides maximum flexibility for new designs.

B&S: So are we talking about a completely new specification here?

Finstel: It is a new specification suitable for many new high-end embedded systems such as virtualized carrier-grade network equipment or IoT edge and fog servers. But it is not entirely new. It is backed up by the highly reliable embedded high-end COM Express Computer-on-Module standard and thus reliable right from the start of the specification release.
B&S: Which interfaces needed to be omitted?

Finstel: Since all the new edge and fog server appliances are headless and don’t need any high-end display support, the Digital Display Interfaces (DDI) on the CD connector were removed to make way for the four 10GbE ports. Type 7 will also support up to 32 PCIe lanes, which is 8 more than on Type 6. To make space for this, LVDS was completely removed and SATA and USB ports where downgraded to 2 and 4 respectively. Finally, the VGA graphics interface was removed to make place for an NC-SI port on the AB connector. NC-SI can be used in combination with either the original GbE port, or with any of the four 10GbE ports.

B&S: What is a typical design example for COM Express Type 7 modules?

Finstel: We see them as a substitute for legacy ATCA platforms and the many proprietary systems in carrier-grade telco networks because technology upgrades are quite expensive due to all these deployed platforms. With COM Express modules, upgrades can be executed parallel to the performance cycles of the latest processor technologies. So I can imagine that performance hungry new telco platforms might get updated annually for the fastest performance hike at the lowest cost. New designs can also have quite a small footprint that is not much larger than the module footprint itself, which is 95x125mm. Add a height of 1U or 2U for the system and you have a very compact embedded server computing box. This is interesting for edge and fog server technology that is hosted by the field application vendor. But we also see rack mount as well as carrier-grade system designs with up to 10 modules in a high-bandwidth 1U system for data-intensive applications with transfer rates of up to 0.4 terabits per system.

B&S: Why Computer-on-Modules in such a complex multi-processor system?

Finstel: Thanks to the modular design with its defined pin out, system design becomes independent of processor technology. Systems can be upgraded by a simple module exchange. This minimizes development costs for performance upgrades and helps to shorten time-to-market. OEMs also gain greater design security and can use their designs for longer, thereby additionally increasing their return on investment.

B&S: When will we see the first COM Express Type 7 module from ADLINK Technology?

Finstel: It’s already here for early field tests and full series production will start at the end of this year. Our new COM Express Type 7 module, the Express-BD7, is based on server-grade Intel Xeon D SoC processors with a TDP of 65 watts or less. It targets customers that are building space-constrained systems in industrial automation and data communication, such as virtualization, edge computing or other numerical applications that require high-density CPU cores balanced by reasonable power consumption. It hosts up to 32GB dual channel ECC DDR4 and supports two 10GbE ports, up to eight PCIe x1 Gen2 lanes, one PCIe x16 Gen3 interface, two SATA 6Gb/s and four USB 3.0/2.0 ports. The module comes with a build option for an extreme rugged operating temperature range of -40°C to +85°C.

B&S: Is COM Express Type 7 backed up by support from processor vendors?

Finstel: COM Express Type 7 only became possible because there is a clear silicon roadmap behind it offering embedded long-term availability!

B&S: OK. That’s great. Now let’s take a look at SMARC 2.0. Why a new interface specification for a standard that already addresses all the new credit card sized small form factor designs based on ARM and x86 technologies?
Finstel: The technology evolves quite fast in this low power to ultra-low power segment and many technologies were not available at the launch of SMARC 1.0 in 2012.

B&S: So are we talking here about something brand new that is designed for entirely different systems?

Finstel: No. SMARC 2.0 is very impressive as well, but it is ‘only’ the successor of SMARC 1.1. The challenge in developing the SMARC 2.0 specification was to integrate the latest features of current SoC platforms while maintaining compatibility with the 1.1 pin out to the widest possible extent. Only pins for interfaces that were rarely used or looked likely to be replaced in the near future by more modern interfaces were allowed to be reassigned. Thus most of the key interfaces supported by 1.1 have not changed in 2.0, and the specification ensures that no damage will occur if a 2.0 module is deployed by accident on a 1.1 carrier board, or vice versa.

B&S: What’s new?

Finstel: Within the new application areas of the IoT, cloud and wireless sensor networks, I first want to mention the -40°C to +85°C extended temperature support for the harshest environments which is a unique feature of all ADLINK Technology SMARC 2.0 modules. Furthermore, dual GbE support as well as the option to design-in antenna interfaces directly on the module is massive innovations in embedded module design. They differentiate SMARC 2.0 significantly from competing module specifications such as Qseven or COM Express Mini. Native support of antennas enables system engineers to design in various wireless interfaces such as 3G or WLAN, or any of the many local wireless interfaces such as Zigbee, LoRaWAN or Sigfox, just to name a few.

B&S: Why is the second Ethernet port so important?

Finstel: Native support of a second Ethernet interface instead of only one is a plus for IoT gateways and process computers with vertical integration, where one Ethernet port connects to the field and the other to the management level. Support of two GbE interfaces also benefits many industrial devices that simply loop this bus through to connect multiple devices in the field, thereby reducing the amount of cabling by allowing the implementation of line or even redundant ring topologies instead of star topologies.

B&S: What other features beside dual Ethernet and wireless support are important to mention?

Finstel: First of all, I would like to say that especially in the context of IoT and cloud services we have a unique feature that differentiates all our SMARC 2.0 and COM Express Type 7 modules from all competing platforms, which is SEMA Cloud support. SEMA Cloud allows all of our latest modules to have native support of cloud services implemented so that OEMs and their customers can access, control, manage and maintain all our boards and modules via cloud servers. And they can use this cloud interface for the entire system. No other embedded computing vendor has such a considerable and consistent offering.

B&S: So your modules can deliver data such as temperatures and power consumption as well as fan speeds and many other health parameters to the cloud?

Finstel: Not only that. We can integrate local peripherals as well and manage OS, firmware and application upgrades or distribute new application data such as sales prices to thousands of devices with only a few clicks. Therefore, IoT connectivity is inherent to our platforms and implemented with the highest security because we designed a dedicated encryption engine into our BMC which makes it more or less impossible to hack our devices.

B&S: The connectivity question seems to be quite comprehensively addressed at ADLINK Technology, which benefits OEMs who already have enough challenges to master with all the new IoT and cloud based applications and services. But I assume that connectivity is not the only feature that makes SMARC 2.0 a next generation module specification?

Finstel: Exactly. Other new features that we have implemented include two MIPI CSI serial camera interfaces. One of them supports up to 4 lanes which is again very interesting for smart digital signage, smart vending machines and smart cameras in smart cities and connected vehicles. And finally, we have also significantly improved the monitor interfaces.

B&S: Which graphics features are new?

Finstel: SMARC 2.0 now also offers dual-mode DisplayPort, a.k.a. DP++, to support resolutions up to Ultra HD/4K with 3840 × 2160 pixels. This interface makes DVI and HDMI displays easier to implement because all that is required is a signal level conversion from TMDS to LVDS. Also, since single-channel LVDS in SMARC 1.1 has become dual-channel LVDS in 2.0, this interface can now drive either two low-resolution displays or one high-resolution display. Depending on which processor is used, the interface can support up to 1920 × 1200 pixels at 60Hz. And since the HDMI/DP interface remains unaltered, developers can connect up to three high resolution digital displays via modern serial display interfaces. Existing carrier boards with single channel LVDS and HDMI can be used with SMARC 2.0 just as before.

B&S: How can we differentiate SMARC 2.0 from Qseven?

Finstel: The new SMARC 2.0 specification offers the latest state-of-the-art interfaces as well as the largest number of interfaces because its MXM 3.0 connector provides 314 pins, which is a lot for such a small form factor. Thus SMARC 2.0 is an ideal platform for highly integrated Computer-on-Modules in credit-card format and we expect that SMARC 2.0 will become the leading SFF standard for both x86 and ARM designs. Qseven addresses the same market but has fewer interface capabilities.
B&S: When can we expect your first SMARC 2.0 Computer-on-Module?

Finstel: The first launch will be with a new processor generation. The new Intel Atom, Celeron and Pentium processors codenamed Apollo Lake are already launched and it is only a matter of weeks before our first SMARC module based on that processor will be available. We couldn’t make it parallel to the launch because the time frame from official specification release in June to the launch date in early September was too short.

B&S: Will SMARC 1.1 modules become obsolete?

Finstel: We don’t think so. All relevant low and ultra-low power processors such as Altera Cyclone V, Xilinx Zynq, Freescale i.MX6, Intel Atom E3800 Series, Intel Celeron N3000, Intel Quark, DMP’s Vortex 86EX, Nvidia Tegra 3 as well as Texas Instruments ARM Cortex A8 and A9 are perfectly suited for SMARC 1.1. Thus we expect that we will have modules based on that specification for many years to come.

B&S: Thanks for all these insights.

Finstel: You’re welcome!

Product News

Axiomtek: 18.5-inch multi-touch panel computer for infotainment
Axiomtek introduced the GOT3187WL-834-PCT, an 18.5-inch fanless multi-touch panel computer for infotainment and light industry applications. The industrial grade widescreen touch panel PC adopts an 18.5") WXGA TFT LCD display with projected capacitive touchscreen and 250 nits high brightness. To provide excellent system performance, the all-in-one touch panel PC supports quad-core Intel Celeron processor J1900 with low power consumption. The 7H surface hardness guarantees superior durability

News ID 4448

Portwell: wide temperature Panel PC with Intel quad-core processor
Portwell announces FUDA2-S1921, a new 19-inch energy-efficient and powerful fanless Panel PC with projective capacitive touch screen. Powered by Intel Atom Bay Trail-I SoC quad-core processor E3845 (10W Max TDP, 2M Cache, 1.91 GHz) integrating Intel Gen 7 3D graphics engine, FUDA2-S1921 provides wide operating temperature support, high I/O connectivity and achieves up to 3x the peak performance and 5x the power efficiency of the previous generation.

News ID 4418

MEN: robust PCIe mini card carrier on CompactPCI Serial
The new CompactPCI Serial carrier board G227 for PCI Express Mini Cards fulfills almost any wish regarding wireless data communication. It offers space for two PCIe Mini Card slots for LTE, UMTS, GSM or HSPA, each with two antenna connectors at the front, one PCI Mini Card slot for WLAN, telephony, GPS or audio signals and up to ten microSIM cards. The versatile PCI Mini Card carrier board G227 is the solution for wireless applications like fleet management or passenger information in the train and other mobile markets.

News ID 4408
Graphics power for high-volume
digital signage installations

By Zeljko Loncaric, congatec

This article highlights the cooperation of semiconductor, computer module and display companies to create powerful digital signage systems at affordable cost.

Digital signage installations are no longer restricted to just a few prestigious applications that require ultimate graphics performance in order to deliver stunning visuals. These days, what matters is being able to offer appealing graphics performance at an attractive price in order to realize high-volume installations. The new AMD Embedded G-Series processors (codenamed Brown Falcon) and its attractive price point now open the door for the mass production of multiple range digital signage solutions.

When using x86-based embedded SoC graphics, it has to be AMD. There is no question about this in the embedded community, even among the fans of other processor makers. The AMD Radeon graphics is without doubt the greatest heavyweight compared to similar competitive solutions. Scalability up to high-end gaming graphics, comprehensive and always up-to-date support of the latest graphics CODECs, plus wide-reaching efforts to continually improve the visual experience of embedded computer applications make the AMD-R-Series processors the choice for graphics-rich digital signage applications.

Perceptual computing, for example, enables us to interact with a system not just via keyboard, mouse or touch, but also through facial expressions, gestures and speech. It is therefore possible to imagine digital signage solutions that can not only count pedestrians and recognize gender but also react to perceived moods. Vending machines might even get a face allowing customers to speak to it as if they were served by a kiosk attendant in person. Many other innovative applications for digital outdoor advertising (often called DOOH or Digital Out of Home) are conceivable thanks to such innovative technologies.

Another key aspect in many digital signage applications is cost. So what do you do, when the performance of the currently available AMD-G-Series processors (Steppe Eagle) is not enough, but the R-Series processors (Merlin Falcon) are too expensive? You choose the new AMD-G-Series processors (Brown Falcon), because they are designed to fill this performance gap. They were developed on the basis of the Excavator microarchitecture, which is also used for the new AMD-R-Series SoCs.

AMD has transferred all characteristics that are relevant for the basic structure and the overall performance of a system from the high-end R-Series processors to the new G-Series processors. However, the feature set was thinned out in favor of a more cost-effective design, which also allows for slimmer and more energy-efficient designs. For example, the G-Series SoCs support only a dual-core version of the Excavator microarchitecture. But thanks to the new boost function, it can be enhanced with an extra shot of performance. This can continue until a specified surface temperature on the die is reached. This is especially important for single-threaded applications, commonly found in digital signage applications - for example in the use of HTML or other web-based content.

For extremely graphics-rich digital signage applications, the new graphics of the G-Series supports two monitors with now up to 4K resolution of 4096 x 2160 pixels at 60Hz. Compared to the previous G-Series, it provides approximately 30% more performance and supports the latest 3D features of DirectX 12 and OpenGL 4.4. This is made possible by the AMD Graphics Core Next (GCN) Generation 3 architecture. While support in the new G-Series SoCs is limited to a maximum of 4 compute units with 64 execution units each, this still adds up to 256 execution units. The G-Series also offers new features for video streaming, which is very important for digital signage applications. For instance, hardware-accelerated decoding of the latest and
most efficient performance-hungry H.265 codec is now supported. In addition, developers can use the integrated AMD Radeon graphics for GPGPU tasks related to perceptual computing, such as the analysis of live audio and video data. Full support of the recently adopted 1.0 specification for Heterogeneous System Architecture (HSA) makes this now easier than ever. With HSA compatible SoCs, developers need to code only once and can then use the same code on different platforms. This streamlines and simplifies programming and there is no need for adaptation to potentially varying heterogeneous resources. This makes dealing with different platform structures very simple. HSA also uses the same memory address space for CPU and GPU, which accelerates the data exchange. The processing power required from the software is automatically allocated to the most appropriate computing units. This leads to optimum performance at minimum power consumption.

Another innovation for the cost-optimized mid-performance range of embedded SoC processors is support of up to 32GB of dual-channel DDR4 RAM with ECC. DDR4 RAM is not only faster but also around 20% more energy-efficient than the previous DDR3 RAM, which has an additional positive effect on performance and power consumption. For applications that require a higher degree of operational safety, or that for instance are exposed to increased radiation, ECC memory modules can be used. This means that bit errors can be corrected automatically in RAM, which significantly increases the application reliability. As far as bandwidth is concerned, it is important to mention that PCI Express
Gen 3.0 is supported. This allows designers to double the data rate over PCIe 2.0 based designs with the same number of lanes. Compared to modules featuring the previous generation of AMD Embedded G-Series SoCs, the dual-core AMD GX 217GI processor provides up to 30% more graphics performance and 15% more overall system performance. At the same time, the maximum configurable TDP remains between 12 to 15 watts, the ideal range for fanless system designs.

congatec has made the new AMD G-Series available on COM Express modules that are also available with R-Series processors to provide a complete family. This makes the new module the first choice for many mainstream applications in the digital signage segment. OEMs also benefit from extremely high scalability up to quad-core performance in the 35 W TDP class that offers game console level graphics performance on up to three independent screens and top class GPGPU performance. Developing solutions ranging from the entry-level to high-end systems with only one module design becomes quick and easy. In the high-performance graphics segment the new conga-TR3 provides best pricing for high-volume applications. The new conga-TR3 COM Express Basic module with Type 6 pin-out is equipped with the dual-core AMD Embedded G-Series SoC GX-217GI processor with 1.7 GHz to 2.0 GHz and supports up to 32GB DDR4 memory, optionally with ECC. The new AMD Graphics Core Next (GCN) Generation 3 architecture controls up to two independent 4K Ultra HD displays @ 60Hz via DisplayPort 1.2 or HDMI 2.0. In safety-critical applications, the integrated AMD Secure Processor provides hardware-accelerated encryption and decryption of RSA, SHA and AES.

The new computer module supports COM Express pin-out Type 6 with 1x4 PCIe 3.0, 1x PEG, Gigabit Ethernet, 4x USB 3.0 / 2.0, 4x USB 2.0, SPI, LPC plus F'C, SDIO and 2x UART. Operating system support is offered for Linux and Microsoft Windows 10, Windows 8.1 and, optionally, Windows 7. Embedded Design and Manufacturing Services for custom carrier boards and a wide range of accessories to facilitate design-in are also offered. As part of its Embedded Design and Manufacturing (EDM) Services congatec offers its customers everything OEMs need. The spectrum ranges from the development of custom carrier boards to complete digital signage systems, which congatec realizes with partners such Technagon, congatec EDM Services start in the design phase with requirement engineering. Services include the development of all specific embedded hardware as well as the required low-level software such as BIOS/UEFI, driver and OS images, ensuring perfect integration into the customer-specific application. Together with the production-ready components from Technagon, full advertising and information systems are designed for optimum manufacturing, both from a technical and economic point of view. Among other things, Technagon covers the display technology, including safety glass and anti-reflective coating technologies required for locations that are prone to vandalism or direct sunlight. The service also covers the entire production cycle and system integration, with the option of including certification and global logistics for delivery at the customers of the customer. OEM customers also benefit from technical system support.

**Product News**

**aceed: 24V PoE switch with 8 insulated gigabit ports**
PoE switches exist in any given numbers. Nonetheless, you need to look for those with a total power output of 120 W. However, the IGPS-1080-24V-I, which conjures up a full 50 W with a maximum of 30 W from a switch cabinet-typical input voltage of only 24 V for all eight Ethernet interfaces, is virtually unique. The inconspicuous abbreviation “I” at the end of the product name expresses a further special feature: all eight ports are insulated (overvoltage protection up to 1.5 kV), and the isolation on the input power side has been enhanced to 1.5 kV.

*News ID 4405*

**Vecow: Skylake-S fanless Embedded workstation system**
Vecow launches her latest high performance embedded box PC with Intel 6th Generation Skylake platform, ECS-9000 Series Fanless Embedded System. With Quad Core Intel 6th Generation Core i7/115/13 processor (Skylake-S), fanless -40 to 75°C operating temperature, all-in-one integrated features, supporting 10G LAN/Fiber, multiple I/O connection, user-friendly, smart manageability, outstanding system performance, excellent mobile availability, 6V to 36V power input with 80V surge protection, ignition power control, intelligent circuit protection and rugged reliability in harsh environments, the ECS-9000 Series Fanless Embedded System is your superb choices for Machine Vision, Intelligent Automation, Smart Manufacturing, Embedded Cloud, Intelligent Surveillance, Vehicle Computing, Mobile Robot Control, and any Industry 4.0 performance-driven real-time embedded computing applications.

*News ID 4449*

**EKF: XMC module carrier supports up to eight PCI Express lanes**
With the SK3-MEDLEY, EKF exhibits a new CompactPCI Serial carrier card for XMC-style mezzanine modules. While using a similar form factor as PMC cards, XMC modules (ANSI/VITA 42/61) are provided with the powerful PCI Express interface. The SK3-MEDLEY is equipped with a PCI Express Gen3 x8 redriver, for optimum high speed signal integrity, and should be installed into a CompactPCI Serial fat pipe slot. The SK3-MEDLEY can be used with 74x139mm² size XMC mezzanine cards.

*News ID 4427*

**ADLINK: COM Express 3.0 type 7 Computer-on-Module**
ADLINK Technology announced its first computer-on-module based on the latest PCI Industrial PICMG COM Express 3.0 specification with new Type 7 pinout, for which ADLINK lead development efforts to bring a server-grade platform and 10 GbE capabilities to a COM form factor. ADLINK’s Express-BD7 targets customers building space-constrained systems in industrial automation and data communication, such as virtualization, edge computing or other numerical applications, that require high density CPU cores balanced by reasonable power consumption.

*News ID 4402*

**b-plus: PC/104-Plus board, perfect for the retrofitting of existing systems**
b-plus offers with its industrial PC/104-Plus PCI04Board DX3 the optimal alternative to discontinued LX800 CPU based products. To reduce costly adaptions and new developments of whole applications and designs, e.g. in industrial machinery, b-plus developed a maintenance free module, that has similar characteristics. It also offers beneficial new features.

*News ID 4362*

**MEN: binary I/O for rail applications on CompactPCI Serial**
The new 3U CompactPCI Serial board G403 with 16 bidirectional digital I/O channels has been designed specifically for modern railway applications. The new board is suited for many different control functions, such as door-locking control and interior lighting. The G403 supports a total of 16 bidirectional digital I/O channels, organized into four optically isolated groups for reliable data transmission with four channels in each group. In addition to an accommodating configuration as either an input or output, each channel features an individual edge-triggered interrupt.

*News ID 4390*
Acceed: programmable I/O module with web interface
Freely programmable I/O modules belong to the core elements in several automation and building technology applications, for mass data processing, in test laboratories and in other industrial processes. The new I/O module RIO-2015PG from Artila, which will already be available from the German distributor Acceed soon, was developed by Artila specifically for this purpose.

News ID 4361

Lanner expands LEC-7230 series IPC lineup
Lanner launches the LEC-7230-CT1, a fanless SFF industrial computer powered by the Intel Celeron J1900 processor, known for its significant improvement in performance and power-efficiency. Benchmark testing conducted for computing performance and power efficiency found that the Intel Celeron J1900 outperforms its predecessor (Intel Atom N2800) by 310% while maintaining the same level of power usage.

News ID 4377

RUTRONIK: update for ATX mainboard D3348-B from Fujitsu
The new version D3348-B2 of Fujitsu’s ATX motherboard D3348-B offers various new features. It addresses customers in need of powerful CPUs on the cutting edge of technology and is ideal for use in CAD workstations, medical equipment and industrial servers in 19” rack format. The update is available at distributor Rutronik as of now.

News ID 4343

IBASE: EN50155 certified Touch Panel PCs for railway applications
IBASE Technology announce the BYTEM-123-PC and the BYTEM-103-PC, both based on the quad-core Intel Atom processor E3845 and EN50155 certified for railway applications. The 12.1” BYTEM-123-PC and the 10.4” BYTEM-103-PC fanless panel PCs provide high computing performance and low power consumption, silently operating at temperatures from -20 to +55°C for BYTEM-123 and -40 to 75°C for BYTEM-103. Meeting EN50155 standards, the units support input voltages including 24V (default) as well as 72V and 110V (options).

News ID 4391

ADLINK: compact fanless embedded computers with 6th gen Intel Core
ADLINK Technology announced the release of its new Matrix MXE-5500 Series, featuring 6th generation Intel Core i7/i5/i3 processors (code name Skylake), and delivering outstanding performance with robust construction, rich I/O, and easy device access, all in a compact package. The MXE-5500 Series sustains reliable performance at -20 to 70°C, shock up to 100G, and vibration up to 5Grrms, making it an optimal solution for ITS, surveillance, and industrial and logistic automation applications. Moreover, AFM (adaptive function module) capability offers fast application-specific access for medium volume operations, reducing development time by up to 50%.

News ID 4344

Artila: Cortex-A5 based industrial embedded Linux computer for remote device monitoring
Artila Electronics releases its Matrix-700, a Cortex-A5 based industrial embedded Linux computer. Matrix-700 comes fanless with long term stability, faster flash memory, flexible input / output function and smaller dimension, etc., powered by a ATME 536MHz ATSAM5D35 Cortex-A5 CPU which is equipped with 512MB SDRAM, 8MB Flash and especially suitable for 24/7/365 non-stop running for unmanned application environment.

News ID 4373

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September 2016

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IRISO’s long-term available MXM2 connector has been qualified for suitability with the third generation of PCI Express. Simulations from EyeKnowHow have proofed that IRISO’s connectors are well suited for use in applications with data transfer speeds of up to 8 GT/s.

MXM2 connectors have been designed to connect graphic cards to motherboards. Now they are widely used for board to board connections in industrial and automotive applications where many signals are to be connected at high data rates. Most popular is the use as a backplane connector for SGET’s popular Qseven module standard. When Qseven was introduced to the market in 2008, SATA2 and PCI Express (“PCIe”) Gen1.1 with net data rates of up to 2.5 gigatransactions per second (GT/s) for each lane were state of the art and PCIe Gen 2.0 was just being introduced to the market after its formal release in 2007. Meanwhile PCIe Gen3 is transferring data at 8 GT/s per lane. While signal transmission at this speed has been established in many embedded systems for quite some time, so far none of the connector manufacturers had committed nor released the suitability for these speeds with their MXM2 connectors predominantly used in Qseven- and graphics systems.

Early this year Japanese connector manufacturer IRISO has got its long-term available MXM2 connector qualified for suitability with the signal transmission speeds which come along with the third generation of PCI Express (“Gen3”). Simulations performed by German company EyeKnowHow have proofed that IRISO’s MXM2 connectors are well suited for use in applications with data transfer speeds of up to 8 GT/s. Specifically, signal transmission in Qseven COM Carrier board scenarios (Device-Up and Device-Down) has been simulated with PCI Express Gen3.

The Standardization Group for Embedded Technology (SGET e.V.) has laid out two generic cases in their Qseven Specification for transmission of data between CPU and connected devices: Device Down, where the target device of the PCIe communication is located right on the main computer board (“baseboard” or “carrier board”), which is connected to the CPU board (here: Computer-on-Module; “COM”) via a board-to-board connector and Device Up, where the target device of the PCIe communication is located on a plug-in module (“AddIn card”) located on the main computer board which is connected to the CPU board. It’s obvious that the second case is more challenging due to the extra discontinuities on the signal path caused by the additional connector.

No need to say that for signal integrity reasons the number of vias has to be kept at an absolute minimum which is defined in the case of Qseven to a number of three pairs (per differential signal) on the CPU module and two pairs on the baseboard. Figures 2 and 3 show the respective simulation setup.

Physical board data for the simulation (Layer stack-up, geometry/routing lengths) have been taken from an actual Qseven V2.0 CPU module and the current reference carrier board and resulted as follows:

- CPU module: routing length: 3” (7.62 mm); with the DC block after 0.3” routing length, impedance 85 Ohms +15% tolerance, Microstrip and Stripline routing, 3 via pairs.
- Carrier board: impedance 85 Ohms -15% tolerance, stripline routing, 2 via pairs.
- AddIn card (Device Up configuration only): routing length 3.5” (8.89 mm), impedance 85 ohms, 2 via pairs.

Simulation purpose was to sweep the in transmission line length to find out the maximum length within a given minimum signal quality at PCI Gen3 speed of 8GT/s and to keep as close as possible to the adopted PCI SIG method. First step was to perform end-to-end simulations of the two configurations (device up/down) from transmit (TX) pad to receive (RX) pad and to determine eye height (EH) and eye width (EW) after reference equalizer at eye pad using statistical methods. Worst case scenarios were applied for mismatches between CPU module and carrier board. Other parameter worst case effects have been adopted by setting margins in eye width and eye height. The simulation was done on base of genuine models from the manufacturer for transmitter, TX/RX package and RX load models. For the channel based on Microstrip (MS) and Stripline (SL) Layout technology the
The simulation followed PCI-SIG rules with adding and optimizing TX-PreEmphasis and RX Equalization settings. As mentioned before, only impedance mismatch effects have been directly included into the simulations. Effects like Corner Case Silicon and others have been lumped into additional margin. For Device Down configurations the defined margin of 20mV (EH) and 15% (EW) can be provided for routing lengths of up to 11” (279.4 mm) on the carrier board plus the 3” (7.62 mm) on the CPU module. For Device Up configurations the defined margin of 20 mV (EH) and 15% (EW) can be provided for routing lengths of up to 6” (152.4 mm) on the carrier board plus the 3” (7.62 mm) on the CPU module and the assumed 3.5” (8.89 mm) on the AddIn card.

In both configurations the simulation shows a non-linear behaviour for eye-height vs. eye-width. The difference between the total routing length shows that the PCIe connector and the additional vias for the add-in card eat up about 1.5” (38.1 mm) of routing length. In practice simulated maximum routing lengths on the base board should be more than sufficient. With real routing lengths being significantly shorter, typical margins will be significantly better than the defined threshold values. Well and efficient routed CPU modules and AddIn cards leave more routing length for the baseboard. The good simulation results with the relatively high share of lumped margin show that the accuracy of the simulation is good enough. Generating more accurate results would require the simulation to be run with exact parameter adjustments for each individual system.

The simulation results for the Iriso IMSA-18010S-230A-GN1 substantiate that this MXM2 connector does its job as baseboard connector for Qseven pretty well and that it has enough reserve for even higher speeds than current PCIe Gen3 with 8 GT/s. The guaranteed 10 year long term availability makes it well suitable for long lasting and long running automotive and industrial applications, too.
IoT opportunity demands new approach to MCU-based embedded designs

By Stefan Ingenhaag, Renesas

The stakes in the IoT market are high. In this hyper-competitive environment, traditional approaches to product development hardly suffice. This article introduces the Renesas Synergy Platform, each element of which, silicon, software, tool ecosystem, kits and reference designs, contributes to a shorter, quicker development cycle.

Let’s face it – the opportunity the IoT market offers is unprecedented. The numbers alone are staggering. Analysts at Gartner Inc. estimate that 4.9 billion connected devices will be in use by the end of 2015, up 30 percent from 2014. Five years from now they expect that number to jump to 25 billion. By then those same analysts expect 10 billion connected devices (excluding PCs, smartphones, and tablets) will ship each year into a market that researchers at IDC forecast to be worth over $7 trillion. At the heart of this exciting new market lies the 32-bit microcontroller (MCU), the source of the intelligence built into the majority of edge devices and hubs across the IoT. As the build-out of the IoT takes off, research firms such as IC Insights are projecting 32-bit MCU sales will grow by a CAGR of 9.5% through 2018.

As an industry-leading manufacturer of MCUs, Renesas offers developers some natural advantages. The company offers prospective customers unparalleled experience in a number of critical vertical markets including medical, home appliances, building automation, factory automation, and energy management. The extensive knowledge base Renesas brings to these markets gives the company unmatched insight into the challenges developers face. And the company value proposition in terms of quality, reliability, support, security and safety is tailored to match customer needs in those markets. But the IoT market is different. One of the toughest challenges the IoT market brings is its impact on the pace of development. Today everyone understands that those who bring their product to market first reap the largest profits. But the advantage of beating the competition to market doesn’t end there. For the most part, today’s IoT market lacks accepted industry standards. Those who get to market first will have the greatest opportunity to influence those standards and gain an edge over the competition.

Second, the IoT market forces embedded developers to reconsider their definition of system-level design. They have to stop thinking of their application as a discrete unit. Instead, they must think in a broader sense about how their application fits into an interconnected world. That, in turn, will force developers to adopt new technologies. As new communications, security, user interfaces and sensing technologies become increasingly commonplace, embedded designers building products for the IoT market must enhance their skills and knowledge of connectivity, the cloud, and portable applications. Most of the MCUs currently in use were never networked in the traditional sense. Few developers have the expertise they need to build those designs.

Most developers will require a deeper understanding of connectivity and security issues and large, complex networks to succeed in the IoT market.

At the same time, universal interconnectivity increases system vulnerability. Security risks lie at each stage of the product lifecycle from manufacturing and development to deployment and remote updates. Most devices connected to the Internet today have inadequate security capabilities. Clearly developers will need a far better command of security and safety technologies to meet customer expectations.

Each of these trends forces developers to devote more time to testing and debugging these new capabilities and to reconsider design priorities. Yet designers face major time and resource constraints as they try to develop new embedded products for an IoT market where product lifecycles are shrinking along with time-to-market windows. In this environment developers who can shorten their product development cycle will likely find more success meeting these elusive market opportunities.

While the IoT market covers a broad field of applications, most require a base set of fundamental capabilities and peripherals.
Complete Medical Embedded IoT/Cloud Solutions

Not only does Microchip have great wireless solutions and eXtreme Low Power (XLP) microcontrollers, we have also partnered with some of the top cloud implementation partners in the business. Microchip products enable end-to-end solutions that help you successfully connect medical devices to the cloud, and take advantage of all of the benefits of doing so.

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To succeed in this market developers will need MCUs that offer an extensive set of communication peripherals, analog I/O, significant on-chip memory and a diverse portfolio of security and safety functions. But the embedded design market already has many semiconductor suppliers offering full-featured MCUs. The key to taking advantage of this coming avalanche of IoT applications will be the ability of each MCU vendor to help lower the total cost of ownership for customers and get development projects to market quicker. To win in the IoT market developers must eliminate many of the low-level, but time-consuming integration tasks they have had to grapple with in the past. Traditionally, developers begin at the silicon level and then have to wade through multiple software and tool options to find the best solution for their particular application. They must spend valuable time evaluating each vendor, understanding their licensing terms and IP acquisition costs. And the work only begins once the developer purchases software or tools. The time and energy developers spend tracking each vendor can be significant. More often than not, each tool, stack and RTOS vendor has a separate roadmap forcing the developer to keep up with the latest releases as they add new features.

At the same time the development team must spend time integrating all of the software components from multiple vendors, then testing and qualifying at the system level to maintain high quality levels while keeping abreast of changes in the marketplace and the latest advances in best development practices. Invariably designers must delay working on the truly differentiated aspects of their design - the end-application code or new features - until the end of the development cycle. In the long run the developer faces enormous uncertainty, the risk of cost overruns and a late entry to market.

The Renesas Synergy Platform is designed to circumvent these obstacles. To minimize cost of ownership and allow developers to begin quickly developing code for their application, the Renesas Synergy Platform treats hardware and software as a single unified product. The benefits begin at the silicon level. The platform is built around a family of compatible and scalable MCUs based on the ARM Cortex-M core. Common features across the MCU portfolio simplify product development. These upwardly compatible MCUs combine extremely low power consumption with a small silicon footprint, an extensive set of peripherals and up to 4 MB of on-chip code flash. To meet emerging IoT requirements, each MCU offers a diverse set of communications interfaces and a broad array of security and safety features.

But the real payoff in terms of lower cost and faster development comes at the software level. Each Renesas Synergy MCU comes with a comprehensive package of qualified software components. Included in the cost of the MCU, the Renesas Synergy Software Package (SSP) features all the crucial software components engineers need to build the basic core system functions essential in any IoT development project. Built around Express Logic ThreadX RTOS, the SSP includes middleware components from Express Logic X-Ware and adds MCU-specific software components such as device drivers, middleware, libraries and a flexible framework with an API.

Each component in the platform is integrated, tested, qualified, scalable and reusable. As a result, designers spend less time on driver implementation, middleware and RTOS inte-
integration and more time focusing on the truly innovative aspects of their design.

The SSP is far different from the typical ad hoc software solution of embedded designers. Developed using industry-accepted best practices the SSP is a qualified software product with an accompanying datasheet documenting measured performance characteristics. The software datasheet for MCUs is an industry first; no other MCU vendor guarantees its MCU software behaviour as specified in a software datasheet. The SSP meets widely accepted standards, tests and benchmarks, such as MISRA and Coremark, as well as published SQA metrics, documented processes and product lifecycle practices. Moreover, Renesas provides full product-level support for the SSP including maintenance with scheduled releases for updates and upgrades, errata publishing and management, issue tracking and bug fixes.

With the Synergy Platform there are lower barriers to getting started; designers can begin development of their end-products much earlier than in the traditional development model. Renesas Synergy Eclipse-based e2 studio integrated solution development environment (ISDE) and the included C compiler are provided free of charge from GNU or the commercial compiler can be purchased from IAR. Engineers can begin full development upon the purchase of any one of many very low-cost development or starter kits available for each of the Renesas Synergy MCU series. Simple registration of the kit automatically grants full rights to develop with the entire Renesas Synergy software package.

The ISDE also brings a new level of innovation in context-aware, real-time assistance through use of integrated smart documentation for software and MCUs. With this new capability engineers no longer need to pore through thousands of individual pages of documentation, saving time and preventing mistakes.

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**Product News**

- **Rutronik: franchise contract with Nanya on SDRAM memory portfolio**

  Nanya Technology and Rutronik Elektronische Bauelemente have concluded a Europe-wide franchise contract, that covers the entire Nanya product portfolio of SDRAM memory. Nanya develops, produces and distributes standard and mobile SDRAM memory. The Taiwanese manufacturer is specifically targeting the automotive and industry markets with its 30nm and 42nm technologies. The 30nm technology offers customers cost and performance benefits such as multi-chip compatibility.
  
  News ID 4350

- **Wuerth Elektronik eSos acquires AMBER wireless**

  Würth Elektronik eSos considerably expands its range in growth fields, such as Internet of Things, Industry 4.0 and Smart Metering. AMBER wireless is one of the leading manufacturers of low power ISM/SRD solutions in Europe and offers highly efficient wireless products in the 169 MHz, 433 MHz, 868 MHz, 915 MHz and 2.4 GHz frequency bands.
  
  News ID 4438

- **Maxim: DeepCover microcontroller enables XAC PCI-PTS 4.1 certification**

  The newest security key pad and smart card readers—E200NP and E200CP—from XAC Automation, which incorporate the MAX32550 DeepCover secure microcontroller from Maxim Integrated Products, have successfully passed the stringent PCI-PTS 4.1 certification requirements.
  
  News ID 4452

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Processors with multiple industrial communication protocols on chip

By Elizabete de Freitas, Texas Instruments

This article introduces the Sitara processors which are tailored for industrial automation and help to form a complete industrial automation platform.

The Sitara processors provide efficient and scalable architectures for the entire Industrial Automation system, using the ARM A-series of cores, including the Cortex-A8, Cortex-A9 and Cortex-A15, all incorporating multiple industrial communication protocols on a single chip. Pin-to-pin and software-compatible devices in each family of processors, along with industrial hardware development tools, software and analog components, provide a total industrial system solution. Using these solutions, developers can get to market faster with their industrial automation designs, including input/output (I/O) devices, human machine interface (HMI) and programmable logic controllers (PLCs).

The Sitara processors combine an ARM A-series core (single or multiple) with the Industrial Communication Subsystem (PRU-ICSS) and typical standard industrial interfaces in a single SoC (System on Chip) to build a differentiated scalable architecture. This unique integration enables small and compact systems, and as they are manufactured in modern silicon technologies supporting lowest power consumption they also enable fanless designs.

The Sitara AM335x processors are the first in the family, and offer the best performance/peripheral integration/price combination. With the ARM Cortex A8 scaling from 300MHz to 1GHz and six pin-to-pin compatible devices with multiple speed grades and temperature ranges, the AM335x devices are the most popular and flexible of all. The ARM Cortex A8 is the first processor supporting the ARMv7-A architecture and has a 2.0 DMIPS/MHz specification offering up to 2000 DMIPs for the AM335x.

The Sitara AM437x processors integrate a high performance Cortex-A9 up to 1GHz that supports single-cycle vector floating point (VFP) offering improved performance for floating point mathematic-intense algorithms such as motor control. The ARM Cortex A9 features an out-of-order speculative issue superscalar execution 8-stage pipeline giving 2.50 DMIPS/MHz providing up to 2500 DMIPs for the AM437x.

The new Sitara AM57x processors feature a unique heterogeneous architecture that includes ARM Cortex-A15 cores, C66x DSPs, Cortex-M4s for maximum performance and scalability. The best computing performance is achieved with two types of cores, one or two ARM Cortex-A15 up to 1.5GHz and one or two C66x DSPs up to 750MHz. Specific control functions can be offloaded to two ARM Cortex-M4 at 213MHz for deterministic, real-time processing. Two ARM Cortex-A15 cores offer 10500DMIPs which can be complemented with 2x C66x DSP cores adding 48 GMACs/24 GFLOPs providing the AM572x family with the highest performance in the Sitara family.

The Industrial Communications Subsystem (PRU-ICSS) is a proprietary subsystem that enables the integration of real-time industrial communications protocols and eliminates the need for an external ASIC or FPGA, reducing overall system cost and complexity. The PRU-ICSS is able to support multiple protocols on the same hardware using firmware supplied by TI, through the Industrial Software Development Kit, and stacks from industry partners. Real-time Ethernet, fieldbus, interface, and redundancy protocols are available for the PRU-ICSS, including certified solutions for EtherCAT, Profinet, Ethernet/IP, SERCOS III, and Powerlink.

In addition the PRU-ICSS include key features like direct access to I/O interfaces, to UART, MI, MDIO and other peripherals. At its core we have a 32-bit RISC engine that can be programmed both in C and in ASM while ensuring 100% deterministic behavior. An additional advantage of the PRU-ICSS compared to fixed function ASIC or FPGA is the ability to upgrade devices deployed in the field with firmware updates.
The AM335x integrates one instance of the Industrial Communication Subsystem – comprising two cores of PRUs – enabling fieldbus/real-time Ethernet or position feedback support. The AM437x integrates one instance of the Industrial Communication Subsystem plus one instance of a reduced Industrial Communication subsystem - providing quad-core PRUs with optimized memory set-up, and enabling one real-time Ethernet protocol and one position feedback protocol for example. The AM57x integrates two full instances of the Industrial Communication Subsystems – quad-core PRUs - which enable multiple protocol options simultaneously including two real-time Ethernet protocols for example.

Starting at field level the AM335x supports scalable ranges of I/O modules with slave communication, where the application is implemented in the ARM core running TI RTOS and fieldbus or industrial Ethernet running in the PRU-ICSS. Also at field level we find industrial drives; these are best implemented in the AM437x combining slave communication on one PRU-ICSS, motor position feedback in the second PRU-ICSS and running the main application and the motor control functions (such as field oriented control) in the floating point optimized Cortex A9. The AM437x enables innovative single chip drives architectures.

Moving up to the control level we see the complete Sitara family supporting Programmable Logic Controllers where the selection of the processor depends on a number of different factors such as the type and number of I/Os. Also key for the selection is the type of master/slave communication needed - important is the software compatibility offered across the different Sitara families, supported with the latest TI integrated Processor Software Development Kit.

At operator level, the AM57x highly integrated platform running TI RTOS or a high level operating system such as Linux offers the best computing performance combined with industrial communication for both slave and master and high performance peripherals such as PCIe for extra connectivity. For video- and graphics-intensive applications, such as human machine interfaces, the AM57x includes video and graphics acceleration cores that enable 1080p60 High Definition video; 2D and 3-D graphics; up to three LCD outputs and one HDMI; and six or more camera inputs.

The Sitara processors are extensively supported by both hardware and software development kits. The TI RTOS Industrial Software Development Kit (SDK) for the Sitara processors gives developers the ability to easily add key functions to automation applications such as: real-time industrial communications, support for motor feedback protocols such as EnDat and a Delta-Sigma Decimation filter; and more. The SDK also includes a real-time, low-footprint SYS/BIOS kernel with boot loader and sample applications to get started quickly. These complement all the hardware features supported by the various scalable hardware development kits.
Improving power supply density and efficiency with GaN power transistors

By Eric Persson, Infineon

For power supply applications requiring higher density, GaN HEMTs enable much higher operating frequency without increasing switching loss. This article describes an LLC circuit which, compared to Si superjunction FETs, operates at 3X higher frequency with no increase in power loss. This combination of factors is necessary to drive power density to higher levels for the next generation of power supplies.

Power supplies today are quite efficient compared to their counterparts 10 or 20 years ago. It is not uncommon for power supplies to feature energy efficiency of >90% over a wide operating range. Premium performance power supplies with 12 or 48 V outputs for server and telecom applications commonly have peak efficiency of 94%, and 96% is also available. And just emerging onto the market are ultra-premium power supplies with peak efficiency of 98%. Clearly the efficiency cannot continue to increase at a linear pace, as it must ultimately asymptote to 100%, a value we will never achieve.

But efficiency is only one aspect of power supply figure-of-merit. The other two key attributes are power density and cost. These three attributes – efficiency, density and cost – balance each other for a particular power supply technology. For example, improving either efficiency or density will come at a price. Or, for a given price-point, increasing efficiency generally comes at the expense of density. Every once in a while, a new technology comes along and shifts this balance, enabling new levels of performance and cost previously not possible. Thirty years ago, it was the silicon power MOSFET that emerged to enable switchmode power supplies with far greater efficiency than the previous bipolar junction transistors of the day could achieve. Silicon carbide Schottky diodes began to make an impact around 15 years ago, and are now widely used as high performance rectifiers in efficient power supplies.

In 2016 it is now gallium nitride (GaN) making high-performance transistors that are again changing the landscape. Specifically, it is enhancement-mode lateral GaN HEMTs (high electron mobility transistors) that are making the biggest difference. Compared to the nearest silicon alternative, the superjunction MOSFET, GaN transistors have far lower charge on the gate and output for a given on-resistance. Moreover, GaN HEMTs have no parasitic body diode. The poor reverse recovery performance of high voltage FET body diodes limits their applicability to topologies that do not require body-diode commutation. GaN HEMTs on the other hand have a diode-like behavior in the reverse direction with zero reverse recovery behavior, so they are ideally suited for high frequency applications, even those requiring body diode commutations.

To begin with, let’s look at the general goals of power supply manufacturers. For all but the most demanding applications, efficiency in the range of 95% is already good enough using actual silicon FETs. The next goal is density, how to shrink the envelope for existing power levels, or more commonly – how to pack more power into the existing size box. The key to improving density is to substantially increase the operating frequency of the power converter. At higher frequency, the magnetic components need fewer turns of copper, less magnetic core volume, and are therefore smaller. Even the capacitors that manage the high frequency ripple current shrink in size. The only capacitors that do not shrink are those required for hold-up time.

But how is it possible to increase frequency without additional switching loss? The answer lies in the control strategy for a particular topology. Regardless of which transistor technology is used, zero voltage switching (ZVS) is one of the keys to minimizing switching loss and enabling higher frequency operation. The majority of power supply topologies are based on the concept of using transistors to switch a voltage source into an inductive load. The goal
of ZVS is to use energy stored in the parasitic capacitance of the switching device along with inductor current to losslessly commutate the switch capacitance, instead of hard-switching where the transistor forces commutation and dissipates the energy stored in the device capacitance. Hard switching is very common in the PFC stage of a power supply. Figure 1 shows the typical boost converter stage switching waveform at the moment the transistor turns on. At $t_0$ the inductor current is flowing through the diode into the bus capacitor. The switch node $V_{sw}$ voltage is therefore at the bus voltage. At $t_0$, Q1 is turned on, and it begins conducting current, which ramps up to the inductor current $I_L$ at $t_1$. Note that the voltage at the switch node $V_{sw}$ has not moved yet. If the diode was perfect and there was no reverse-recovery charge, then the switch node voltage would begin to move towards zero at $t_1$. But if D1 is a PN junction diode (or the body diode of a synchronous rectifier), then the diode cannot immediately stop conducting, so the current in Q1 continues to ramp up, as does the corresponding reverse current in the diode. This continues until $t_2$, when the diode recovers its ability to block voltage, and stops conducting. At this point, there is a significant reverse recovery current on top of the steady state inductor current, and the transistor Q1 is supporting this peak current while simultaneously supporting the full bus voltage across its drain-source. This leads to the high peak power dissipated in Q1 during the turn-on interval, as shown by the $P(t)$ curve (which is the product of device current times voltage) peaking at $t_2$.

Finally, between $t_2$ and $t_3$, the current through Q1 discharges the capacitance of the switch node and drives the voltage to zero, thus dissipating the energy stored in the diode capacitance and Q1’s own self-capacitance. To summarize, in a hard-switched turn-on, there are 3 main energy loss mechanisms each cycle. 1) Commutation or crossover loss: proportional to current risetime. Faster turn-on means lower loss. 2) Reverse recovery loss (does not apply for Schottky diode), depends mostly on the diode characteristic. Diodes with large $Q_{rr}$, like the body diode of a superjunction FET, can have extremely large $Q_{rr}$ and completely dominate the turn-on loss. 3) $E_{oss}$ loss: this is the energy stored in the capacitance of the switch node (including the switch itself, the diode, and parasitic capacitance in the inductor) that gets dissipatively discharged each time the switch is turned on.

As a simple example of zero voltage switching (ZVS), consider the same boost PFC circuit as in the previous example, except this time the control strategy is different. Instead of continuous conduction mode (CCM), the current is allowed to reach zero each cycle. Of course this means that the ripple current of the PFC stage...
is a much higher magnitude (and therefore the RMS current and corresponding conduction loss is increased), but allowing the inductor to fully discharge sets up the condition for lossless commutation of the diode – essentially free ZVS.

The example in figure 2 shows the process. When the inductor current reaches zero, the equivalent circuit is an LC, where the capacitance is not the big bulk capacitor on the DC bus (it is blocked by the diode), but the combined output capacitance of the switch plus the parasitic capacitance of the diode and inductor. The initial condition of the circuit is that C is charged to the bus voltage, and at t0, it will resonate and ring down to negative bus voltage, only the switch will clamp it as it crosses zero volts. This mode of operating the PFC circuit is known as critical conduction mode CrCM. The concept of using small amounts of energy stored in the inductor or in device capacitance is widely used to enable ZVS in a variety of topologies and control strategies. The LLC converter (figure 4) is a good example of a DC-DC stage that uses resonance to achieve ZVS in the back half of a power supply. As already mentioned, ZVS can work with any type of switch, but here is where the big difference between conventional silicon FETs and GaN HEMTs becomes important. The far lower capacitance and charge of the GaN HEMT requires less energy and shorter dead-time to achieve ZVS, compared to silicon FETs. The shorter deadtime is the main reason that LLC can now be operated at much higher frequencies without incurring additional loss.

Normally in the LLC circuit, the ZVS transition only takes a small percentage of the total resonant period – for example it may be 330ns out of a typical operating frequency of 150 kHz, approximately 5% of the period. But if the frequency were increased 4X to 600 kHz, now the 5% (per edge) becomes 20%! The transition time (also known as deadtime) is non-productive power transferring time – it is simply waiting for the lossless ZVS transition. This means that, as the deadtime becomes a larger percentage of the total period, the productive portion of the resonant period is proportionally smaller, and this drives the RMS current much higher due to the higher peak to average ratio.

In other words, in order to increase frequency significantly in a ZVS circuit, the circulating energy required to achieve ZVS has to decrease proportionally, otherwise the penalty of increased RMS current on both the primary and secondary sides will kill the efficiency of the power supply, making it impossible to improve density. But the relationship between capacitance, charge and energy in modern high voltage (superjunction) MOSFETs is complex because the capacitance is so

### Table 1. Typical parameters of 600 V superjunction FET compared with 600 V GaN HEMT.

<table>
<thead>
<tr>
<th></th>
<th>For 55 mΩ nominal Rds(on)</th>
<th>Best Superjunction</th>
<th>E mode GaN HEMT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Qg (typ)</td>
<td>68 nC</td>
<td>6 nC</td>
<td></td>
</tr>
<tr>
<td>Qoss (typ)</td>
<td>420 nC</td>
<td>44 nC</td>
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<tr>
<td>Eoss (typ)</td>
<td>8 μJ</td>
<td>7 μJ</td>
<td></td>
</tr>
<tr>
<td>Qrr (typ)</td>
<td>6,000 nC</td>
<td>0 nC</td>
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nonlinear. This not only makes it difficult to compare devices based on datasheet capacitance values (as they can change 3 orders of magnitude depending on voltage), but also makes a big difference between devices that are optimal for hard switching (low Eoss), versus ZVS soft switching (low Qoss). The graph in figure 3 clearly illustrates this difference. A 650 V, 70 mΩ rated high performance superjunction FET is shown in blue, compared to a GaN HEMT with the same rated on resistance in red. The dotted lines indicate charge (left axis), and the solid lines indicate energy, both versus Vds voltage on the horizontal axis.

Note that the superjunction charge (dotted blue line) rises steeply up to 90% of its final value within the first 20 volts applied. The slope then abruptly changes so the final 10% charge takes the remaining 380 volts. This is a result of how the charge distributes in the columnar structures of a superjunction FET. This behavior has an interesting effect: since the energy required to pump charge into the Coss at low voltage is smaller due to the V2 relationship ($E = \frac{1}{2} CV^2$), even though 90% of the charge occurs in the first 20 volts, a far smaller portion of the total energy is stored by this point. This characteristic nonlinearity is why superjunction FETs can have a relatively low Eoss for a given Qoss, and therefore is what makes them excellent (low Eoss) for hard-switching applications compared to the other silicon alternatives.

In stark contrast, the GaN HEMT is a lateral device and has a low, nearly linear capacitance versus voltage. In figure 3, the red dotted line shows this as a shallow slope rising to a value an order of magnitude smaller than the superjunction Qoss. But since this charge is evenly distributed along the voltage axis, the integration of charge times voltage brings the final value of Eoss almost the same as the superjunction. This relationship is summarized in table 1, comparing Si superjunction FET to a GaN HEMT. The HEMT is still better in Eoss, but by a much smaller margin than Qoss where it is 10X improved. To further illustrate the effect of Qg and Qoss, the well-known LLC circuit of figure 4 is used to evaluate the ZVS performance of both devices. The same circuit is used for comparison of both Si and GaN on the primary side running at approximately 350 kHz, delivering 750 W from a 385 V bus.

Figure 5a shows the waveforms for the superjunction FETs on the primary of the LLC, and figure 5b shows the GaN HEMT in the same circuit, same conditions. In figure 5a, the upper gate turns-off and the drain voltage takes more than 350 ns to slew from bus to zero volts. The superjunction nonlinear charge creates long, shallow tails on the voltage that mandate the long deadlock. As shown, the deadlock in Figure 5a is 350 ns, and even then, when the lower gate turns-on, the voltage has not yet reached zero (so it is near ZVS). This may seem to be a small compromise, turning on slightly early before the voltage across the switch is really zero, but it is not: don’t forget that nearly half the Eoss still remains at only 20 V on the drain because of the nonlinearity (refer to figure 3 blue Eoss curve). In other words, the deadlock shown is as short as it can be without significant compromises in power loss (and efficiency).

Figure 5b shows the same waveforms for the GaN HEMT. Note that the gate voltage has a much faster rise and fall time than the superjunction device. This is a result of the gate driver having a much easier time driving the low charge gate of the GaN device. Moreover, due to the low Qoss of the HEMT, the drain voltage is linear and much faster as well. Because of this, the deadlock can be 3X shorter, and have no additional loss from non-ZVS.

A real-world LLC example: figure 6 shows two LLC power supplies. They are both 3 kW telecom supplies operating from a 385 V DC bus. Both were designed for high efficiency, and their efficiency curves are nearly identical, hitting peak efficiency of 98.3%. The difference is that the power supply on the left is operating at nominally 130 kHz using superjunction silicon MOSFETs on the primary side, and silicon low voltage MOSFET synchronous rectifiers on the secondary side. The power supply on the right is operating at 350 kHz using 600 V GaN HEMTs on the primary side, and silicon synchronous rectifier FETs. Because of the ~3X higher operating frequency, the GaN power supply on the right achieves 140 W/in3, nearly 3X higher density than the 50 W/in3 standard Silicon-based power supply on the left.

The key to increasing power density is to operate at higher frequency, MHz instead of 100 kHz. This reduces the size of magnetic components and puts them in a range where circuit-board integration is feasible—in other words integrating the windings into the PCB and using planar core structures that can be machine-inserted. Including the windings on the PCB also helps minimize the termination effects that cause hot-spots on conventional magnetic structures. Termination effects occur when all of the AC current sums into a connection point between the magnetic and the PCB. Even if the transformer is manufactured with Litz wire, it has to be soldered at some point, and that is where the skin-effect makes the losses really high. With PCB winding on the other hand, the synchronous rectifier and capacitor components can be literally mounted right on the winding, completely eliminating the termination losses, and additional losses due to parasitic impedance. This technique can work at power levels from a few watts up to several kW. At higher power levels, the transformer is generally divided into several segments like a matrix transformer. Each transformer element can operate at power levels up to 500 watts or more. The primaries are placed in series (to ensure current sharing), and the rectified secondaries are placed in parallel to sum the current just as they are on the toroidal transformer pair in figure 6 right.
LoRA wireless networking standard opens up the smart city

By Simon Duggleby, RS Components

This article describes the advantages of the long range LoRa network for creating IoT applications, not only in cities but also spreading into the rural environment.

The Internet of Things (IoT) is a revolution in the way technology enables countless different systems to work together. It uses the free flow of data to democratise technology and let new types of business evolve and disrupt traditional suppliers by reducing costs and improving service. Like the IoT that it serves, the LoRa wireless networking standard is showing that it can harness the same driving forces and help unleash greater technological creativity.

Rather than wait for telecommunications companies to build an IoT network, The Things Network encouraged organisations and inhabitants spread around Amsterdam to create their own in the space of just six weeks using the LoRa technology. Thanks to its long range, the group was able to cover much of the city with just ten gateway routers. Now the group has turned its attention to other cities around the world, helping them to build a wireless infrastructure for the IoT that will be free of the subscription charges used by operators for conventional networks based on cellular radio.

The LoRa protocol was originally developed by the integrated-circuit (IC) supplier Semtech to operate on unlicensed RF bands such as the widely supported 868 MHz band in Europe. To help spread use of the technology, Semtech has licensed the technology to IC manufacturers Microchip and STMicroelectronics. The protocol uses a spread-spectrum modulation scheme that ensures communications between gateways and devices do not interfere with each other. Spread-spectrum coding creates a set of virtual channels that increase the communications capacity of each gateway. The possible and probable emergence of multiple network operators is not an issue for LoRa thanks to its use of spread-spectrum to separate not just individual packets but communications to and from different gateways within the same area.

The coding scheme lets devices choose the most appropriate data rate for them without affecting devices using other virtual channels. This helps optimise not just network capacity but maximises the battery life of sensor-node devices. The data rate of a LoRa link can range from 0.3kbit/s to 50kbit/s using a protocol that dynamically adapts the transmission rate. Devices can sit at distances of at least 15km from a gateway for line-of-sight communications or up to 5km where line-of-sight is not available, such as in dense urban environments. Several layers of encryption are available to protect data and ensure that messages to and from critical infrastructure can be transmitted securely across open, multi-tenant networks. Different key pairs operate at the network level, the application and device level, to allow security needs to be fine-tuned. In contrast to cellular technology where the operator must carefully manage cell overlap, with LoRa a message transmitted by an end device can be received by one or more gateways. Every gateway that receives the message will forward it to the network – servers deal with any duplication and ensure that replies are delivered to the target application in the cloud. Servers in the cloud can use not just point-to-point communication to talk to end devices but can also take advantage of multicast packets to send commands to groups of devices efficiently, allowing for a wide range of application use cases.

One of the first use cases developed for the Amsterdam network was a service to prevent boats sinking in one of the many canals of the city. The core of the idea is a water detector installed on the floor of the boat. If the boat starts to fill with water, it can send a message to a server that then alerts the owner by a text message to their phone. Replying "clear my boat" would then send a service to check and repair the boat before the water level causes it to sink under the surface.

The severe flooding that Calderdale — an area in the North of England — suffered in recent years, provided the motivation for setting up a Things Network community to build a LoRa
WAN network for the area. The long-range technology allowed for many more flood network sensors than a simpler wireless technology with a far shorter range, or sensors that made use of commercial cellular networks for backhaul.

The Things Network is planning to run other proofs of concept that range from crowd-funded solar electricity generation to keeping track of garden tools. The peer-to-peer lending service Peerby, for example, wants to run a trial on the Amsterdam network that will let users check where implements they have lent to other service users are being used or stored. WeShareSolar wants to connect the solar panels it installs to the network to let users monitor the electricity production of them all in real time. And QvikSense aims to use sensors to monitor temperature, humidity and carbon dioxide levels in buildings to help reduce sick leave. In the UK, Reading is one of the cities also set to benefit from the ability of communities to come together to provide wireless network services. TTN Reading has performed end-to-end tests of the network and early adopters have initiated projects such as performing on-the-fly signal strength measurements around the city, as well as one to attach tiny transceivers to hedgehogs to provide researchers with information on their movement and development. Another idea is to use the LoRa network to support smarter car alarms. Instead of unnecessarily waking up neighbours when the car detects a possible intruder, a device in the car attached to the alarm could send text alerts direct to the owner instead.

The openness of the LoRa means there will be many more options for IoT wireless wide-area networks. Early in 2016, German start-up Digimondo, working together with Semtech, organised a demonstration of LoRa-enabled IoT applications at the influential Embedded World exhibition in Nuremberg. The south German city became the latest in a list of rollouts that started with Hamburg and Berlin and will later extend to rural coverage of the country. In the demonstration, LoRa gateway received messages from vehicles driving around Nuremberg, letting visitors track their locations in real time on monitors installed on the Semtech and Microchip booths. One of the key reasons for Digimondo electing to base its IoT network on LoRa was to help improve communication with its initial focus on smart meters, many of which are often installed inside buildings and may also be underground. The LoRa signal is able to penetrate far enough below ground to communicate with buried devices such as water meters. Magnetic parking sensors are also likely to benefit from the reach of the LoRa protocol.

As LoRa extends from cities into the rural environment, farmers may choose to add their own gateways to the network. Agriculture is one of the many activities that can benefit from the widespread use of sensors. Sensors that monitor the temperature of soil or crops as well as environmental conditions such as pH can help farmers determine where and when to irrigate and to identify areas where pesticide or herbicide applications need to be focused. The long reach of LoRa signals will allow even big farms to gain coverage using only a few gateways on even large tracts of land. At the same time, they can provide wireless IoT infrastructure to their neighbours in villages that otherwise would not have an affordable connection.

Thanks to its open nature in which communities can become operators of their own infrastructure, LoRa is enabling the IoT to deliver on its promise to supply applications that can create smart cities. And, thanks to the long range of LoRa, that smartness can easily spread into the rural environment.
This article highlights how secure interfaces, secure gateway, secure network and secure processing can protect the connected car against cyberattacks, and allow its users to be in full control of their data, making the connected car an opportunity for business and society, rather than a threat to us all.

The automotive industry is rapidly evolving and the car is being transformed from a simple mode of transport to a personalized mobile information hub. All these electronic functions bring great benefits to the driver, increasing comfort, convenience, safety and efficiency. But these features come with new risks, too. Modern vehicles are gradually turning into smartphones-on-wheels, which continuously generate, process, exchange and store large amounts of data. Their wireless interfaces connect the in-vehicle systems of these connected cars to external networks such as the internet, enhancing consumer experience by enabling new features and services. But this connectivity also makes the connected car vulnerable to hackers who attack the vehicle by seeking and exploiting weaknesses in its computer systems or networks. This fact, there are various attackers, with different motivations, skill levels and resources. For example, there may be (academic) researchers who try to take (partial) control over the vehicle, for scientific reasons. Or there may be (organized) criminals with large budgets that want to steal valuable data from a vehicle, for financial gain. Traditionally, there has been a strong focus on safety, meaning that for example the brakes should function correctly under all circumstances. Safety will remain equally important in the future, but the increasing amount of electronics and software in vehicles will additionally require security, to protect the vehicle against hackers.

In 2015, vehicle hacks reached the popular press, with the Jeep and Tesla, and caused some of the biggest vehicle recalls in history. For the first time, the public started to understand the need for increased in-vehicle security. US politicians felt the need to get involved and most recently the FBI have decided the risk is so high, they have even issued warnings to the public. But the events of last year have also shown the world that different OEMs had different security levels in place already, and different speeds of solving the issue. Most vehicle hacks consists of a number of smaller steps. It usually starts with finding vulnerability (a bug) in a system that is remotely accessible. But once you get for example into a car...
internet-of-things
telematics unit, you have a good chance of getting into just about any other part of the car such as the ECUs that control engine speed, braking, cruise control, valet parking etc. It is good practice to use multiple security techniques to mitigate the risk of one component of the defense being compromised or circumvented. Implementing a framework of 4 security layers will lead to a highly secure vehicle network:

To secure the connected car, one has to start with the external interfaces themselves. First of all, the communication channels need to be protected against data theft, e.g. by encrypting the data, and against manipulation, e.g. by authenticating the messages that are exchanged to protect their authenticity and integrity. Furthermore, the interfaces need to prevent unauthorized access. This involves processes such as machine-to-machine authentication to check that you are communicating with a known or authorized device.

As we saw with last year’s Jeep hack, once hackers obtain access to a network, they can send messages anywhere. This is where layer 2, the secure gateway, plays its part. A central gateway ECU separates the TCU and OBD from the network and breaks up the vehicle network into functional domains, with the gateway firewall deciding what nodes can legitimately communicate with a known or authorized device. In the Tesla Model S hack of 2015, the protection offered by the secure gateway is a critical requirement, but on its own may not be enough to stop hackers. For example, they could compromise and impersonate a trusted device and use this to bypass access control. Therefore, one has to apply additional lines of defense. One logical place to do so is in the in-vehicle network, which forms the spine of the vehicle and connects all the different parts of the brains (ECUs). For example, countermeasures may need to be implemented on the network level. Once the external interfaces and internal networks are secured, the brains of the connected car must also be protected. These brains are formed by up to (and in some cases, over) a hundred individual computers (ECUs) that together implement the control functions in the car, including many advanced (automated) driving functions. These ECUs continuously generate, process, exchange and store large amounts of valuable (sensitive) data. And this protection helps in different ways:

1) Prevention of access, e.g. using machine-to-machine authentication and gateway firewalls, to ensure that hackers cannot access and tamper with the safety critical nodes in the vehicle.
2) Detection, e.g. secure boot of the controller, to validate that the software is genuine and trusted.
3) Reduction of impact, e.g. by isolating the network domains, to prevent a compromised infotainment unit being used to control e.g. the brakes.
4) Fixing vulnerabilities e.g. enable full vehicle OTA update capability through the secure gateway, to fix vulnerabilities before they can be exploited (at large scale) by hackers. The connected car, as part of a smarter world, is highly connected and constantly interacting with its environment. In a new era of vehicle complexity and connectivity, these connections bring enormous promises for increased comfort, safety and efficiency. But with that there opens a new era of ingenuity and resourcefulness for car hackers, as with all connected devices, and the connected car becomes a target for cyberattacks. The security of the vehicle electrical architecture is vital to ensure the safety of the vehicle occupants. To secure all of this, an integral approach is needed where countermeasures are applied at all levels. The exact security requirements for a specific vehicle need to be determined using a thorough risk analysis that must be part of its design process.

The four layers of automotive security

The four layers of automotive security

Layer 1: Secure Interface
Secure N2M authentication, secure key storage

Layer 2: Secure Gateway
Domain isolation, firewall/filter, centralized intrusion detection (IDS)

Layer 3: Secure Network
Message authentication, CAN ID killer, distributed intrusion detection (IDS)

Layer 4: Secure Processing
Secure boot, run time integrity, OTA updates

u-blox: automotive grade qualified positioning and connectivity modules

u-blox announced the expansion of its product offering with automotive qualified product variants added to their range of positioning and cellular wireless connectivity modules. The additions comprise the NEO-M8Q-01A and NEO-M8L-01A, and respectively the SARA-G350-02A and LISA-U201-03A. Manufactured according to the ISO/TS 16949 automotive supply chain quality management standard, the modules are thoroughly tested with an extended qualification process aimed at achieving the lowest level of failure rates.

News ID 4368
FPGA expertise for signal processing in portable ultrasound devices

By Jürgen Kern, NetModule

As a vital means of clinical imaging diagnosis, ultrasound examination plays a key role in veterinary medicine. Anesthesia is not required so many diseases of the internal organs can be quickly detected, and the results of professional animal breeding checked. Portable analytical devices for real-time image display are less intrusive for both humans and animals.

US company E.I. Medical Imaging is rapidly taking a lead in this market with its Ibex ultrasound devices for vets and professional animal breeders. These devices enable swift determination of the fertilization phase and can verify pregnancy at an early stage. In developing the Ibex devices, E.I. Medical relies on the FPGA expertise of NetModule. The latest generation - Ibex EVO - had to overcome a particular challenge with the interaction between the software, the Xilinx FPGA, the system CPU, data transmission using SerDes technology as well as the real-time processing of ultrasound signals all the way to the presentation of the imagery.

In addition to its system design expertise in realizing circuitry logic, NetModule applied its professional competence in the real-time processing of rapid image signals such as ultrasound using powerful FPGAs. At the heart of the Ibex ultrasound imagery unit is a signal processor realized in FPGA. This high-performance FPGA core provides an ideal platform for the exceptionally high signal-processing throughput required in order to realize basic functional elements.

These include the beam former for calculating the high-resolution ultrasound beams from numerous parallel receiver channels, the signal processing chain for filtering, envelope detection and signal enhancement, as well as the scan converter for converting polar or rectangular scan formats into a standard video-compatible format.

This Ibex EVO device generation, too, uses the largest chip from the most cost-effective Xilinx product line. This is important as the ultrasound scanners are destined for sale in a price-sensitive market. Whereas a Spartan3A DSP served as the core of the first generation, the Ibex EVO uses an FPGA from the Artix7 family, which enables much more powerful signal processing that provides images of unprecedented quality on a portable ultrasound device of this type.

Ultrasound technology calls for extensive and CPU-intensive signal processing, which means that the number of available DSP cells in the FPGA is key. A DSP cell contains a hardware multiplier and two adders. At the cycle frequency of 160 MHz applied here, this type of cell can perform 160 million multiplications and 320 million additions per second. However, the FPGA chip contains a large number of these cells: where the first generation consisting of the Ibex Lite and Ibex Pro products with the Spartan3A DSP chip (model 3400A) used 126 of these arithmetic units, the new 2nd generation Ibex EVO with the Artix7 (model 200T) features no less than 740 DSP arithmetic units. This enables a higher number of additions per second, accordingly. For the Ibex EVO ultrasound devices, this allowed the number of channels for sending and receiving to be increased from 16 to 64. As a result the display of ultrasound images benefits, while sharpness and contrast increase in line with the number of channels used. This, in turn, enables a larger display format in SVGA image quality.

The second hurdle was to realize the connection of the transducer to the FPGA. After all, 64 signal channels also require 64 analog-to-digital converters. In this case, NetModule opted for the relatively new SerDes technology that is capable of transmitting data at 3.2 GBit per connection. The system consists of a serializer/deserializer - for the serial transmission of parallel data. The parallel data to be transmitted is converted in the serializer into a serial data stream with a high bit rate. It is then transferred serially, and reconverted again in parallel in the deserializer for further processing. (Source: Wikipedia)

The system also features a function that sets it apart: the Ibex Evo scanners can be used to show the flow of blood in the body. This technology, known as Doppler Ultrasound and Colour Doppler, is based on the physical phenomenon of the Doppler effect: if sound
transmitters and receivers move towards or away from one another, runtime delays are created. This can be exploited in medicine to show movements of bodily fluids (e.g. blood). Movements towards the ultrasonic transmitter are usually overlaid in red, while movements away from it are overlaid in blue (- Colour Doppler). (Source: Wikipedia)

This latest Ibex EVO generation is equipped with a sealed 8.4" (approximately. 21.33 cm) LED display and a backlit keyboard. The complete digital image is always clearly visible even in sunlight and shows unprecedented quality for such a portable and robust ultrasound device. The device displays all modes — B, B+M, PD and colour. The scanners are portable and can operate independently of the mains supply (battery operation). Weighing a mere 2.8 kg, these ultrasound devices are true lightweights that are ready for immediate use.

Their batteries supply power for more than 3 hours and can easily be replaced while the device is in use. Since animals are examined in their natural surroundings, the scanners must function in harsh environments, both in sunshine and rain as well as in dirty environments, and they must also be waterproof and easy to clean.

Thanks to DuraScan technology, they are not only shockproof and dustproof but also biologically safe. In other words, they pose no risk to the animals being examined. In addition to swift results and the high degree of precision, the devices impress with their cost efficiency and longevity (EVO converters have survived 1.2 million load cycles in use). Vets can check their results directly, thus saving valuable time.

Product News

**Mouser: CY8CKIT-143A PSoC 4 Bluetooth module minimizes design time for BLE development**
Mouser Electronics is now shipping the CY8CKIT-143A PSoC 4 BLE 256K module from Cypress Semiconductor. This fully certified Bluetooth Low Energy module is an easy-to-use solution for creating a complete BLE system with Bluetooth 4.2 features — data length extension, upgraded privacy, and enhanced security — all of which are critical for Internet of Things applications. The module’s compatibility with Cypress’s small-footprint (10×10×1.8mm) CYBLE-222014-01 Bluetooth 4.2 module makes it ideal for medical, home automation, and wearables applications.

News ID 4395

**TME: IoT and wearables development platform**
An interesting solution for designers specializing in wearable electronics and Internet of Things has just entered the market. NXP Semiconductors and MikroElektronika jointly created the Hexiwear platform that transforms the approach towards designing breadboards. The device has the looks and size of a digital watch. However, it offers a far greater functionality than features commonly connected with smartwatch products. As a complex, open project platform, Hexiwear allows you to create and test your applications using six built-in sensors of the device.

News ID 4370

**IBASE collaborates with Microsoft to accelerate IoT solutions**
IBASE Technology has joined Microsoft Azure Certified for Internet of Things, ensuring customers get IoT solutions up and running quickly with hardware and software that has been pre-tested and verified to work with Microsoft Azure IoT services. Microsoft Azure Certified for IoT allows businesses to reach customers where they are, working with an ecosystem of devices and platforms, allowing for faster time to production.

News ID 4413
Intelligent vision systems enable totally new eras in robotics

By Fredrik Bruhn, Unibap

Intelligent vision systems are key in one aspect of the three technological trends fuelling the evolution of robotics: high resolution sensors, powerful heterogeneous system architectures (HSAs), and highly efficient brushless DC motors. HSAs like the AMD G-Series SoC offer highly integrated processor architectures in a unified platform.

The ability to comprehend is no longer limited to the animal kingdom; machines are increasingly able to recognize, manipulate and influence the world around them. Technological trends have created the right environment to support advanced robotic systems that now play a crucial role in modern life. The range of applications for robotic systems is vast, as they move from automating the manufacturing process to being the hands and eyes of highly experienced surgeons. The potential for robots to aid an ageing population cannot be overlooked.

Fundamental to these robotic extensions of ourselves will be three key technologies, which are now advanced enough to support what some are already calling the robotic revolution. First comes vision; machine vision systems are now enabled by low cost, high performance sensors that provide much greater resolution than those of even just a few years ago. Next comes the ability to process the data generated by these advanced sensors, an area where massive advancements have been made in recent times, especially in the area of executing deep learning algorithms. Lastly comes movement; here, the great leaps that have been made in the development and efficiency of brushless DC motors provides the third key enabler for advanced robotics. Spatial awareness, enabled through stereoscopic vision, is so natural in the animal kingdom that it makes perfect sense to adapt the same principle for machines, which has given rise to the intelligent vision system. In this application, two high resolution camera sensors provide stereoscopic visual data which is then processed by high performance digital processors. Such systems are now being used with robot arms in assembly applications, while the same technology is fuelling the burgeoning automotive vehicle industry. Acting as the eyes to robotic systems, intelligent vision systems must now perform a large amount of the data processing closer to the sensors, before passing the processed information on to the main system. This is made necessary because of the large amount of data now being generated by vision sensors, and made possible thanks to the advances made in processor technology. An intelligent vision system would once have been simple frame grabbing with perhaps some pixel binning, performed by a digital signal processor, at the time the most efficient engine for complex algorithms requiring parallel processing.

Creating this artificial visual cortex requires a combination of advanced digital processing platforms. Thanks to their parallel nature and hardware efficiency, FPGAs are used for processing individual pixels straight out of the sensors. Like the human eye, cameras have evolved to see in color; red, green and blue (RGB), encoded to display information in a way suitable for the human eye. For intelligent vision systems, this representation is less useful than hue (the color circle), intensity (old grey scale) and saturation (how much color or grey) (HIS) and so the first task for a vision system is to convert RGB data into HIS data (using a computer, this conversion could require one core per sensor, but using an FPGA there is almost no area penalty and a delay of just six processing clock cycles).

Vision systems commonly employ lenses to improve their effectiveness, while the use of fish-eye lenses is becoming more common to further extend their field of view. Correcting for the effects of lenses is the next process and at this stage the two images will also be matched to create the stereoscopic image. This processing is typically carried out in the FPGA, while all subsequent processing would be handled by a heterogeneous SoC, such as the AMD G-Series SoC. It is through advances in HSA design, like those found in the AMD G-Series SoC, that they become suitable engines for
emerging intelligent vision systems. By building on established designs, decades of research and evolutionary artificial intelligence, HSAs provide the ideal platform for the next generation of machine vision systems.

The complexity involved with understanding the world through images should not be underestimated. The vision systems found in nature have evolved over millions of years, yet their digital counterparts have only been in development for mere decades. Nevertheless, software running on advanced processing platforms can now be seen as comparable in its ability to tackle this complex challenge. Neural networks have been in use for many years, but recent leaps in processing power mean their use is no longer compromised by the platform’s ability to match their potential, enabling the adoption and development of even bigger and, more importantly, much deeper (more layered) neural networks. Indeed, while limitations in processing power meant neural networks may have needed to be simplified in the past, modern SoCs are more than able to support highly complex networks with many layers.

Other forms of artificial intelligence are also seeing the benefits of more powerful processing architectures. A leader in this field is x86 architecture, which has always been at the forefront of adopting new technologies. It successfully combines instructions optimized for streaming and vector operations, developed over many years, with new technologies such as Shared Virtual Memory. All of these innovations are employed in the latest heterogeneous system architectures, which allow software engineers to make full use...
of the hardware features in a single, unified environment. The latest generation of AMD SoCs represents how the theory of HSA is put into practice. Heterogeneous processing platforms essentially combine processors with different architectures in a single device, which AMD refers to as the Accelerated Processing Unit (APU). This brings together the powerful x86 CPU and its ability to efficiently execute sequential programming, with its highly optimized Graphical Processing Unit (GPU) designed to tackle parallel processing. By harnessing the potential of the GPU for intelligent vision systems, the HSA delivers greater power efficiency and, therefore, a total increase in processing capability.

The software ecosystem for advanced applications like intelligent vision systems also benefits from the HSA approach. Open standards such as OpenCV (Open Source Computer Vision) and OpenCL (Open Computing Language) make software development much simpler and so harnessing the power of an HSA less challenging. Developers can create advanced software applications without needing to focus on partitioning code between the various processing elements in an HSA; the platform and low level software has been developed to help with code partitioning and execution, in order to get the highest performance. This allows many powerful and complex algorithms to be efficiently ported to an HSA.

As intelligent vision systems develop and are deployed in significant numbers to enable the next generation of robotics, society will rapidly come to rely on them. Perhaps the most apparent of these applications will be autonomous vehicles, but their use will be widespread. Their safe operation will be imperative and the integrity of the data stored essential, because decision making (a fundamental feature of advanced robotics) will rely heavily on the integrity of the data available. There would be no human operator present to blame, for example, if an accident occurs due to the malfunction of a care-giving robot.

Highly dense integrated devices are increasingly prone to the phenomena know as single event. These occur when a single ionizing particle comes into contact with a transistor or other integrated element causing a change of logic state. The result, termed a single event upset, can change logic 0 to logic 1 in a memory device, for example, thereby changing the way a piece of code executes or, in other words, the decision an intelligent system makes. Protecting against the effects of single events is taken extremely seriously by the aerospace industry due to the potential consequences and, in part, to the closer proximity of the electronic systems to the cause: cosmic particles colliding with atoms in the atmosphere. While the probability of a single event occurring varies between systems, they could potentially occur once every 100 hours of operation. Protecting against the effects of single events hasn’t been a high priority for most applications outside the aerospace industry, but for machine vision systems it could become so.

Independent tests carried out by the NASA Goddard Space Flight Center have demonstrated that the AMD G-Series SoC can withstand a total ionizing radiation dose of 17 Mrad(Si). This compares favorably with the specification normally applied for standard space flights, of just 300krad. While a single event could hit anywhere, integrated memory such as SRAM is most susceptible due to its high density, while its importance to code execution is apparent. AMD employs advanced error correction (ECC RAM) in the G-Series SoCs, which is able to compensate for the effects of single events. This makes the G-Series even more applicable to intelligent vision systems.

The development and deployment of robotic systems is set to extend beyond industrial automation to all vertical industries. Intelligent vision systems are a key component of that evolution, forming one aspect of the three technological trends fuelling the evolution of robotics: high resolution sensors, powerful heterogeneous system architectures (HSAs), and highly efficient brushless DC motors. HSAs like the AMD G-Series SoC offer a highly integrated and powerful combination of processor architectures in a unified platform. When coupled with open source software ecosystems, developers are empowered to create solutions that allow more advanced deep-learning algorithms to be used, moving machine vision systems and robotics from a sense-compare-decide model to a sense-plan-act behavioral scheme. Machine vision systems like the intelligent vision system IVS-70 from Unibap, enabled by the AMD G-Series SoC and Microsemi SmartFusion2 FPGA, demonstrate how advanced integrated devices and software are coming together with high performance optical systems to deliver machine vision solutions that will empower the robot revolution.

Figure 2. Time synchronization is perfect at the microsecond level, even if the computer screen can show only milliseconds. Picture taken with a 10 Mpix stereo-pair (2 x 5.2 Mpix) of 70 mm lenses.
COG: XML-based smartPCN-Standard simplifies handling of change notifications

A drastic reduction of the manual efforts concerning Product Change Notifications (PCNs) of all kinds are guaranteed by the smartPCN-specification Release 2.0 developed by the industrial association Component Obsolescence Group (COG) Deutschland. The latest XML-based machine-readable smartPCN communication format disposes of a universal and flexible design enabling a mostly automatic handling of change notifications along the entire supply chain, ranging from the single components level up to final applications.

News ID 4463

EVT: box volume measurement with EyeVision 3D

EVT presents the new 3D EyeVolume measurement system with the Bluetechix Time of Flight sensor and the new user interfaced based on the EyeVision image processing software. The Time of Flight 3D scanner measures the volume of boxes and other containers. For this the EVT team has created with the EyeVision Process Mode Layout Editor a user interface for the easy-handling of the EyeVolume commands.

News ID 4428

SEGGER: J-Link Firmware upgrade for BBC micro:bit

SEGGER has introduced J-Link support for the BBC micro:bit providing students a path to using a production grade IDE for their next micro:bit project. SEGGER offers the capability to upgrade the firmware on the BBC micro:bit DAPLink to a J-Link OB (On Board). This firmware makes the on-board debug solution on the BBC micro:bit compatible to J-Link, allowing users to take advantage of all J-Link features such as ultra-fast flash download and debugging speeds and the free-to-use GDBServer as well as application development using an IDE.

News ID 4439

GrammaTech’s team TECHx places second in DARPA’s Cyber Grand Challenge

GrammaTech and its partner the University of Virginia took second place in DARPA’s Cyber Grand Challenge finale, showcasing next-generation technologies for software vulnerability discovery and application hardening. GrammaTech’s team competed with Xandra – its high-performance, scalable system that harnessed 2400 cores to power 210 high-performance fuzzing pods capable of 1.8M fuzzing ops per second and feeding a dedicated bank of binary analyzers, patch generators, and binary rewriters to repair and protect binaries.

News ID 4419

Express Logic: new sales and support office in France

Express Logic has established a sales and support office in France. With this office, located about 35 kilometers southwest of Paris, Express Logic will better serve the growing numbers of local developers using its ThreadX RTOS and middleware products and generate new business throughout the country.

News ID 4415

NI: LabVIEW 2016 new channel wires simplify development

NI announced LabVIEW 2016 system design software, empowering engineers to simplify development and effectively integrate software from the ecosystem into their systems. The latest version of LabVIEW introduces new channel wires to simplify complex communication between parallel sections of code. Available on both desktop and real-time versions of LabVIEW, the channel wire method helps improve code readability and reduces development time.

News ID 4424
Rohde & Schwarz and Promate: global strategic framework agreement for display solutions

Rohde & Schwarz and Promate have expressed the mutual interest for a long-term collaboration on an important material group by signing a global framework agreement for the development and delivery of display solutions. Displays, which increasingly include touch functionality, represent an important human-machine interface for end-users of test & measurement and communications equipment. Rohde & Schwarz has successfully partnered with this industrial Taiwanese Specialist for some time.

Express Logic receives Microsoft exFAT licensing approval

Express Logic is licensed to make and distribute the Microsoft Extended File Allocation Table (exFAT) file system. With this exFAT licensing, the first earned by any RTOS provider, Express Logic offers exFAT file support in its FileX file management system for distribution to customers. Introduced in 2006, the Microsoft exFAT file system is an enhanced alternative to the File Allocation Table (FAT) file system and New Technology File System (NTFS). Microsoft exFAT enables embedded developers to manage larger file sizes than they could with the FAT file system and requires less overhead than NTFS, making it ideally suited for Express Logic’s target markets.

Express Logic: memory cards, eUSB and memory cards

EUSB and memory cards, provides a new level of product differentiation targeting the industrial and embedded markets. ATP will showcase these new solutions and related products at the Flash Memory Summit 2016.

Infineon: highly integrated Hall sensors by Infineon reduce systems costs considerably

The new Hall sensors of Infineon Technologies enable automotive, industrial and consumer electronics to meet strict environmental standards. Also, they help fulfill the requirements of very cost-effective and compact designs. The Hall sensors of the new TLx496x family are highly integrated, have precise switching points, a stable operation and a low power consumption. They are available as latch and switch-type sensors.

Gemalto: cloud data security still a challenge for many companies

Despite the continued importance of cloud computing resources to organizations, companies are not adopting appropriate governance and security measures to protect sensitive data in the cloud. These are just a few findings a Ponemon Institute study titled “The 2016 Global Cloud Data Security Study,” commissioned by Gemalto (Euronext NL0000400653 GTO. The study surveyed more than 3,400 IT and IT security practitioners worldwide to gain a better understanding of key trends in data governance and security practices for cloud-based services.

Gemalto: cloud data security study still a challenge for many companies

Axiomtek: mini-ITX motherboard with multiple high-speed I/O

Axiomtek has launched MANO500, its first mini-ITX motherboard based on 14nm 6th generation Intel Core i7/i5/i3 and Pentium processor in the LGA1151 socket with Intel H110 chipset. The embedded motherboard supports up to 32GB of speedy DDR4 RAM, and offers three SATA connections.

More information about each news is available on www.Embedded-Control-Europe.com/magazine
You just have to type in the “News ID”. —
Cadence launches Tensilica Fusion G3 DSP
Cadence Design Systems announces the availability of the new Tensilica Fusion G3 digital signal processor, a multi-purpose, high-performance DSP ideal for compute-intensive system-on-chip designs. The Tensilica Fusion G3 DSP is exceptionally easy to program and ideal for use in automotive, consumer, internet-of-things and industrial applications that combine intensive audio, imaging, communications, radar and embedded DSP computation. The Tensilica Fusion G3 DSP expands on the multi-purpose Tensilica Fusion DSP product family introduced in 2015.

News ID 4379

Silicon Labs: sensor-to-cloud developer kit accelerates IoT design
Silicon Labs has introduced a cost-effective prototyping vehicle that makes it easy to connect wireless sensor nodes to mobile devices and the cloud to help businesses make data-driven decisions. Silicon Labs’ new ‘Thunderboard React developer kit features a battery-powered, sensor-rich demonstration board with Bluetooth low energy technology and a powerful ARM Cortex-M4 processor for IoT connectivity, along with open-source design files and software for mobile apps running on Android and iOS devices.

News ID 4375

HCC Embedded acquires networking business of InterNiche Technologies
HCC Embedded has acquired the networking business of InterNiche Technologies. Through this acquisition HCC has created a global, combined business that streamlines and simplifies the development of networking and storage solutions for Internet of Things devices. Effective immediately HCC assumes responsibility for providing legacy and technical support to users of InterNiche networking software.

News ID 4372

SEGGER and Renesas: collaboration accelerates expansion of RX ecosystem
Renesas and SEGGER announced their collaboration to facilitate expansion of the ecosystem of Renesas’ RX Family of 32-bit microcontrollers through adoption of SEGGER’s newly-released SystemView software. Forthwith SystemView will support streaming over J-Link, as well as real-time analysis and visualization, in relation to any Renesas RX-based embedded design.

News ID 4366

Phaedrus: RTOS visualisation for Micrium’s µC/OS-III
Phaedrus Systems announced that Percepio, the Swedish developer of RTOS visualization tools, has launched Tracealyzer for Micrium’s µC/OS-III with streaming trace. The new Tracealyzer for µC/OS-III is built on Percepio’s latest Tracealyzer 3.0 platform and contains its streaming trace recorder, which allows for capturing arbitrarily long trace recordings as well as the traditional snapshot (RAM buffer) recorder. The new Tracealyzer for µC/OS-III is an easy upgrade for licensed users of µC/Trace.

News ID 4341

SYSGO announces ELinOS version 6.1 industrial grade Linux
SYSGO introduces version 6.1 of its industrial grade Linux operating system ELinOS, which has been optimised for real-time embedded applications. The new version of ELinOS is based on Linux Kernel 4.1 with real-time extensions, support for ARM 64bit architecture, as well as the X86 64-bit. ELinOS 6.1 enables developers, with a minimum working knowledge of Linux, to quickly build a development environment for Internet of Things and industrial applications.

News ID 4339

Advantech: in-vehicle network video recorders certified for continuous monitoring of fleets
Advantech will be demonstrating their application-ready building blocks for satellite navigation seconded video processing solutions at InnoTrans. They are designed, pre-tested and verified to build video data based fleet monitoring and surveillance solutions – including local video analytics such as movement detection and recording storage – as well as live video based infotainment systems that offer augmented reality functions like adding house numbers or location-based advertisements in real-time to the video stream.

News ID 4464

Acromag: AcroPack I/O platform with reconfigurable Xilinx Artix-7 FPGA
Acromag’s new APA7-200 series provides a user-customizable FPGA on an AcroPack mezzanine module. The module plugs into a connector on an AcroPack carrier to add up to 48 TTL or 24 EIA-485/422 I/O signals or a mix of both types. Mix and match I/O combinations in a single slot for embedded applications running on Linux, Windows, or VXWorks operating systems.

News ID 4389

ARBOR: digital signage player supports 4K/ultra HD display
ARBOR Technology presents its new ELIT-1850, a fanless digital signage player that supports 4K/ultra HD resolution content. The ELIT-1850 is powered by 5th generation Intel Core i7-5650U/13-5010U processors built on 14nm process technology, and supports up to 8GB 204-pin DDR3L SODIMM system memory.

News ID 4369
Microchip: end-to-end security for IoT devices connected to Amazon Web Services’ Cloud

Microchip announces the industry’s first end-to-end security solution for Internet of Things devices that connect to Amazon Web Services IoT (AWS IoT). Microchip and AWS collaborated to develop this integrated solution to help IoT devices quickly and easily comply with AWS’ mutual authentication IoT security model. Using Microchip’s new security solution will help companies to implement these security best practices from evaluation through to production. The solution adds a high level of security, simplifies the supply chain, and is now one of the fastest ways to connect to the AWS Cloud.

ST expands STM32L4 series and introduces development ecosystem

STMicroelectronics has introduced the development ecosystem for its latest low-power, high-performance STM32L4 microcontrollers and expanded the series with five new product lines comprising a range of package and memory-density options. The expanded STM32L4 ecosystem builds on ST’s free and easy-to-use STM32Cube platform. This comprises the STM32CubeMX initialization-code generator and configurator with easy-to-use power estimation for ultra-low-power design, and the STM32CubeL4 package that contains middleware components, Nucleo-32 Board-Support Package, Hardware Abstraction Layer, and Low-Layer APIs.

ROHM: 16bit MCUs optimized for rechargeable NiMH applications

LAPIS Semiconductor, a member of the ROHM group, has announced the development of the ML620130 family of 16bit low power MCUs, optimized for compact industrial equipment requiring battery drive in noisy environments, featuring superior processing capability with low power consumption.

Arrow Electronics signs global franchise agreement for Cypress’ IoT portfolio

Arrow Electronics will distribute Cypress Semiconductor’s newly acquired Internet of Things portfolio, comprising state-of-the-art Wi-Fi, Bluetooth and ZigBee RF technologies capable of connecting nearly every emerging product category in the IoT ecosystem – including home appliances, health and fitness monitors, automation and asset tracking systems, smart meters and an array of consumer electronics devices.

Avalue: fanless embedded system with stable 24/7 operation for IoT and Industry 4.0

Avalue brings the HPC-BYT embedded system to the market to catch the trend of IoT development. This new machine is featured with Intel Bay Trail platform to meet the requirements of IoT-relevant applications including exceptional video and graphics performance, high speed data processing with low power and low profile design. In addition, with the concern of the possibility of industrial or demanding applications, HPC-BYT is also given with rugged features to secure a continuous and smooth operation.

ADLINK: IoT gateway line expands support for Intel IoT Gateway Technology

ADLINK announces the release of three ADLINK IoT gateway models supporting Intel IoT Gateway Technology. The MXE-110i, MXE-202i, and MXE-5400i, based on the Intel Quark, Intel Atom, and Intel Core processors, respectively, further expand the scope of ADLINK’s IoT gateway-based scalable computing platforms.

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STMicroelectronics has introduced the development ecosystem for its latest low-power, high-performance STM32L4 microcontrollers and expanded the series with five new product lines comprising a range of package and memory-density options. The expanded STM32L4 ecosystem builds on ST’s free and easy-to-use STM32Cube platform. This comprises the STM32CubeMX initialization-code generator and configurator with easy-to-use power estimation for ultra-low-power design, and the STM32CubeL4 package that contains middleware components, Nucleo-32 Board-Support Package, Hardware Abstraction Layer, and Low-Layer APIs.

Microchip: end-to-end security for IoT devices connected to Amazon Web Services’ Cloud

Microchip announces the industry’s first end-to-end security solution for Internet of Things devices that connect to Amazon Web Services IoT (AWS IoT). Microchip and AWS collaborated to develop this integrated solution to help IoT devices quickly and easily comply with AWS’ mutual authentication IoT security model. Using Microchip’s new security solution will help companies to implement these security best practices from evaluation through to production. The solution adds a high level of security, simplifies the supply chain, and is now one of the fastest ways to connect to the AWS Cloud.

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Express Logic’s high performance RTOS and Middleware is easy-to-use, making your development job easier and more likely to end up on time or even ahead of schedule. Find out how our products can help you bring your next electronic product to market faster than your competition.
Creating sustainable IoT success
Making the Internet of Things smart, secure and power-efficient

The right technology brings IoT business models to life and ensures ease-of-use, reliable performance and security. From a technical perspective, IoT business models across industries rely on the smart aggregation and interpretation of data. This data is provided by individual “smart” objects equipped with semiconductors, such as sensors, processors, security controllers and actuators. At Infineon, we strengthen our customer’s IoT business models and partner with them to become more successful: Because our semiconductors make the IoT smart, secure and power-efficient.

Our core competencies are essential to create sustainable IoT success for our customers

**Advanced sensing capabilities**
- More than three billion integrated sensors sold over past 10 years
- Special packaging technologies, dedicated processes and robust sensing elements to withstand the harshest conditions
- Break-through innovations such as 3D image sensor for Gesture Control

**Trusted security protection**
- Hardware-based security as a trust anchor
- End-to-end, easy to implement
- Tailored to the application

**Cross application control**
- Cross-domain expertise and systems understanding
- Strong processing and steering know-how from decades of MCU market leadership for industrial, automotive and multimarket applications

**Efficient power management**
- Reduced energy consumption due to highest power density
- Increased power performance by smart power management
- New opportunities due to digital power innovations

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