When Speed matters: From Board to Board with PCI Express Gen3 at 8 GT/s

By Hans-Joachim Jahn, IRISO

IRISO's long-term available MXM2 connector has been qualified for suitability with the third generation of PCI Express. Simulations from EyeKnowHow have proofed that IRISO's connectors are well suited for use in applications with data transfer speeds of up to 8 GT/s.

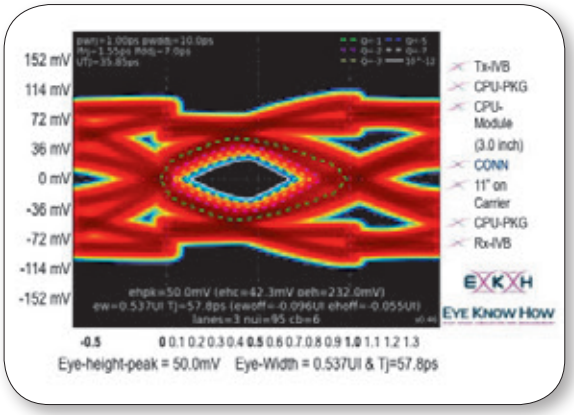

Figure 1, The Eye diagram shows the final result of the connector simulation with 11" routing length on the carrier board in Device Down configuration, i.e. without further AddIn card on the carrier board.

■ MXM2 connectors have been designed to connect graphic cards to motherboards. Now they are widely used for board to board connections in industrial and automotive applications where many signals are to be connected at high data rates. Most popular is the use as a baseboard connector for SGET's popular Qseven module standard. When Qseven was introduced to the market in 2008, SATA2 and PCI Express ("PCIe") Gen1.1 with net data rates of up to 2.5 gigatransactions per second (GT/s) for each lane were state of the art and PCIe Gen 2.0 was just being introduced to the market after its formal release in 2007. Meanwhile PCIe Gen3 is transferring data at 8 GT/s per lane. While signal transmission at this speed has been established in many embedded systems for quite some time, so far none of the connector manufacturers had committed nor released the suitability for these speeds with their MXM2 connectors predominantly used in Qseven- and graphics systems.

Early this year Japanese connector manufacturer IRISO has got its long-term available MXM2 connector qualified for suitability with the signal transmission speeds which come along with the third generation of PCI Express („Gen3"). Simulations performed by German company EyeKnowHow have proofed that IRISO's MXM2 connectors are well suited for use in applications with data transfer speeds of up to 8 GT/s. Specifically, signal transmission in Qseven COM Carrier board scenarios (Device-Up and Device-Down) has been simulated with PCI Express Gen3.

The Standardization Group for Embedded Technology (SGET e.V.) has laid out two generic cases in their Qseven Specification for transmission of data between CPU and connected devices: Device Down, where the target device of the PCIe communication is located right on the main computer board ("baseboard" or "carrier board"), which is connected to the CPU board (here: Computer-on-Module; "COM") via a board-to-board connector and Device Up, where the target device of the PCIe communication is located on a plug-in module ("AddIn card") located on the main computer board which is connected to the CPU board. It's obvious that the second case is more challenging due to the extra discontinuities on the signal path caused by the additional connector.

No need to say that for signal integrity reasons the number of vias has to be kept at an absolute minimum which is defined in the case of Qseven to a number of three pairs (per differential signal) on the CPU module and two pairs on the baseboard. Figures 2 and 3 show the respective simulation setup.

Physical board data for the simulation (Layer stack-up; geometry/routing lengths) have been taken from an actual Qseven V2.0 CPU module and the current reference carrier board and resulted as follows:

■ CPU module: routing length: 3" (7.62 mm); with the DC block after 0.3" routing length, impedance 85 Ohms +15% tolerance, Microstrip and Stripline routing, 3 via pairs.
■ Carrier board: impedance 85 Ohms -15% tolerance, stripline routing, 2 via pairs.
■ AddIn card (Device Up configuration only): routing length 3.5" (8.89 mm), impedance 85 ohms, 2 via pairs.

Simulation purpose was to sweep the in transmission line length to find out the maximum length within a given minimum signal quality at PCI Gen3 speed of 8GT/s and to keep as close as possible to the adopted PCI SIG method. First step was to perform end-to-end simulations of the two configurations (device up/down) from transmit (TX) pad to receive (RX) pad and to determine eye height (EH) and eye width (EW) after reference equalizer at eye pad using statistical methods. Worst case scenarios were applied for mismatches between CPU module and carrier board. Other parameter worst case effects have been adopted by setting margins in eye width and eye height. The simulation was done on base of genuine models from the manufacturer for transmitter, TX/RX package and RX load models. For the channel based on Microstrip (MS) and Stripline (SL) Layout technology the

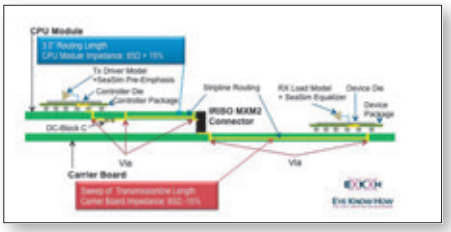

Figure 2. Simulation Setup for Device Down Configuration

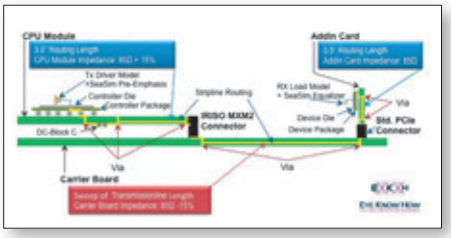

Figure 3. Simulation Setup for Device Up Configuration

layer-stack corresponding MS/SL multilayer models were used. Models for the vias have been created with a momentum field solver.

The Iriso Qseven connector model was generated by port combining and de-embedding out of physical measured s-parameter data. After combining of IL, RL, FEXT and NEXT data with the ADS touchstone combiner utility the final result was a 12 port connector model. While top and bottom side performance was comparable, due to slightly higher insertion loss the topside data were selected for channel simulation. With top-to-bottom crosstalk being less than -50dB at 4 GHz three differential pairs have been used on one top. The s-parameters for Device Up simulation with the assumed standard PCIe connector have been provided by the vendor.

The step response transient simulation has been executed with ADS using the CPU vendor models as drivers with the step response being captured at the RX pad at the end of the channel. In the next step the step response waveforms of the victim and two aggressors have been saved and fed into the simulator for statistical eye calculation.

The simulation followed PCI-SIG rules with adding and optimizing TX-PreEmphasis and RX Equalization settings. As mentioned before, only impedance mismatch effects have been directly included into the simulations. Effects like Corner Case Silicon and others have been lumped into additional margin. For Device Down configurations the defined margin of 20mV (EH) and 15% (EW) can be provided for routing lengths of up to 11" (279.4 mm) on the carrier board plus the 3" (7.62 mm) on the CPU module. For Device Up configurations the defined margin of 20 mV (EH) and 15% (EW) can be provided for routing lengths of up to 6" (152.4 mm) on the carrier board plus the 3" (7.62 mm) on the CPU module and the assumed 3.5" (8.89mm) on the AddIn card.

In both configurations the simulation shows a non-linear behaviour for eye-hight vs. eye-width. The difference between the total routing length shows that the PCIe connector and the additional vias for the add-in card eat up about 1.5" (38.1 mm) of routing length. In practice simulated maximum routing lengths on the base board should be more than sufficient. With real routing lengths being significantly shorter, typical margins will be significantly better than the defined threshold values. Well and efficient routed CPU modules and AddIn cards leave more routing length for the baseboard. The good simulation results with the relatively high share of lumped margin show that the accuracy of the simulation is good enough. Generating more accurate results would require the simulation to be run with exact parameter adjustments for each individual system.

The simulation results for the Iriso IMSA-18010S-230A-GN1 substantiate that this MXM2 connector does its job as baseboard connector for Qseven pretty well and that it has enough reserve for even higher speeds than current PCIe Gen3 with 8 GT/s. The guaranteed 10 year long term availability makes it well suitable for long lasting and long running automotive and industrial applications, too. ■

Config on Carrier Board	Length Variation	Eye Height (abs) [mV]	Eye Height (abs) [UI]	Eye Height (Margin) [mV]	Eye Width (Margin) [UI]
Device Down	10"	56.4 mV	54.3%	31.4 mV	24.4%
Device Down	11"	50.0 mV	53.7%	**25.0 mV**	23.7%
Device Down	12"	44.2 mV	53.1%	19.2 mV	23.1%
Device Up	5"	50.7 mV	48.8%	25.7 mV	18.8%
Device Up	6"	46.5 mV	46.9%	**21.5 mV**	16.9%
Device Up	7"	41.0 mV	46.2%	16.0 mV	16.2%

Figure 4. Simulation Results Summary: The required Eye Hight margin of at least 20 mV can be kept while not exceeding 11" (Device Down) respectively 5"(Device Up) routing length on the carrier board. Eye Width margin of min. 15% is not critical here.