System design enablement and verification for the IoT

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This article introduces some new additions to the Cadence Verification Suite, which makes it the go-to solution for verification and software development for designs in the new age of the Internet of Things.

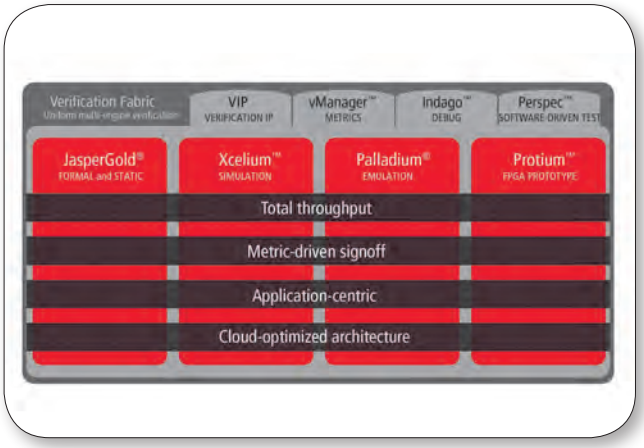

Figure 1. The Cadence Verification Suite

■ Spanning across most application domains, the internet of things (IoT) changes the requirements and priorities for hardware/software development, extending them well beyond the classic considerations of just performance, power and cost. Integrated verification - smartly combining formal verification, simulation at the transaction and classic register transfer level (RTL) - emulation and FPGA-based prototyping have become key requirements. The Cadence Verification Suite already led the way with best-in-class engines for formal verification and emulation. In February 2017, Cadence rolled out next-generation releases for simulation and FPGA-based prototyping. The Cadence Xcelium Parallel Simulator introduces the next era of simulation with true multicore parallelism, integrating technology from the 2016 Rocketick acquisition. The Protium S1 FPGA-based prototyping platform marks a new milestone by further reducing the time to prototype from months to days. It offers congruency with emulation and unique new features for software development, previously unknown to FPGA-based prototyping. With these new additions, the Cadence Verification Suite becomes the go-to solution for verification and software development for designs in the age of IoT. Designs labelled as IoT are applicable from wearable electronics connected to mobile devices, through smart homes connected to set-top boxes, the connected car including driver assistance and car-to-car connections, all the way to enterprise automation for smarter industrial, healthcare, city and energy management. They include designs for the edge node, like our fitness trackers and sensors in industrial automation, and designs for the hubs that aggregate data, like our cell phones, cars and home automation systems, as well as very complex designs for networking and servers in which data is transmitted and analyzed, enabling never-before-seen applications through machine learning and big-data analytics.

While in the past power, performance and cost were the main drivers helping design teams to prioritize designs, in the age of IoT they are now joined by other priorities like security, connectivity and in-field upgradeability. Not only are there more priorities to consider and properly balance, they also change depending on the end application. For fitness trackers, for instance, cost is highest priority, followed by power and connectivity. In contrast, for in-body health implants like defibrillators or cochlear implants for improved hearing, security and safety become the highest priority as nothing can go wrong in a device like this, ever. In-field upgradeability comes second—surgeries should not be repeated—followed by energy consumption. In reactive applications for automotive, industrial automation and robotics, performance comes first, followed by connectivity and in-field upgradeability. A lagging response in a car warning to the driver can easily put human life at stake or risk large revenue loss when industrial production may be brought to halt. Within the city infrastructure, for items like traffic lights or city-wide installations of important control functions, in-field upgradeability becomes the highest priority due to the volume and distribution in the field, followed by security of the infrastructure and cost.

Given the varying development needs for edge nodes, hubs, networks and servers, trying to meet varying priorities across multiple application domains, the vehicles for verification and software development need to be extremely flexible and require close interaction. Figure 1 shows the Cadence Verification Suite with its four core engines of formal, simulation, emulation and prototyping. It is crucial for development teams to be able to efficiently move a design through the different engines, and to capitalize on the individual strength of the engines by optimally combining them. A verification fabric spans across the engines and provides a unified user experience for key tasks like verification management, debug and portable testing. In combination, engines and fabric are geared to

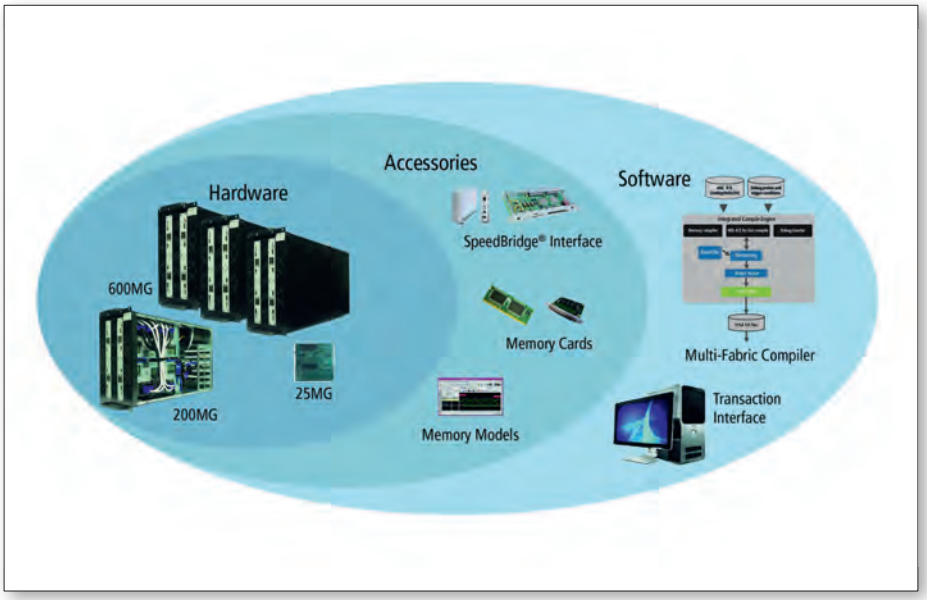

Figure 2. Cadence FPGA-based prototyping portfolio

optimize total throughput for designs, allowing fastest time-to-market and to allow metric-driven design, giving developers a clear indication when they are ready to proceed and roll out their products. The resulting software development and verification flows are optimized for specific application domains, such as adding specific capabilities around functional safety and ISO 26262 compliance for automotive, and are architected to be remotely accessible through cloud-based design.

Focusing in on the hardware engines, emulation and FPGA-based prototyping have long been available to accelerate speeds, extending the range of verification into hardware/software verification, software development and system validation. In the era of IoT, software development clearly has become the long pole in the tent, gating time to product delivery, and with that time, to revenue. Being able to develop software early and in parallel to hardware has become key to product success and requires the speed of hardware-assisted development.

Emulation, typically in the MHz range, is classically focused on high-value use models extending hardware verification to low-power optimization, performance analysis and even early verification of test sequences for post-silicon verification, all enabled by simulation-like debug, fast bring-up and very flexible allocation of tasks in emulation farms. With its higher speed in the tens of MHz or even 100MHz, the FPGA-based prototyping sweet spot has classically been software development and system validation. Neither engine has been without challenges. Emulation has always been somewhat speed-limited, and while smart connections to virtual platforms in hybrid setups can dramatically accelerate the time to point of interest by 50X, FPGA-based prototyping generally achieves the appropriate performance that satisfies the needs of software developers. However, time to prototype, due to the largely manual optimizations required and the need to re-write the RTL to make it FPGA friendly, has traditionally been long, often taking months.

The Protium S1 platform, together with the Cadence Palladium Z1 Enterprise Emulation Platform, directly addresses these challenges and revolutionizes bring-up time by an average of 80% from months to weeks or even days. It gives users the fastest path to prototype for software development, system validation and hardware regressions.

To enable this, the key innovations delivered in the Protium S1 platform are on the level of automation, enabling fastest time to prototype and its congruency with emulation. Designs that run in emulation through the Cadence multi-fabric compiler will come up in weeks or even days when mapped to the Protium S1 platform. No RTL changes are required, partitioning and memory compilation is fully automated, and FPGA place and route is fully integrated. Bottom line, the manual efforts that traditional prototyping requires are fully automated and users typically see designs running at 3MHz to 5MHz out of the box, around five times faster than in emulation. But that's not where performance stops. The platform is scalable from 3MHz to 100MHz, from fully automatic to fully manual. It's automated front-end allows further optimization of clocking, critical paths and memory ports. Together with higher effort place and

route, this easily extends the speed range to 10MHz. To extend performance even further, the Protium S1 hardware can replace home-grown FPGA systems easily and, with manual optimization, allows them to get to tens of MHz performance. For software development, the platform offers very specific, unique capabilities not found in any other FPGA-based prototyping systems. Memory upload and download together with capabilities to freely start and stop the design, and force and release signals, enable advanced software debug. It also has a transaction interface that allows host-based software to be connected. It is scalable from single-board designs to two, four and eight FPGA configurations scaling from 25 million gates to 200 million gates per chassis. It features multi-user support and scales to multiple chassis to 600MG and more.

To cover a wide range of design sizes and accommodate different i nterface r equirements, the Protium S1 platform comes in multiple hardware configurations, r anging from two FPGAs per system to eight FPGAs per system. All FPGAs are Xilinx Ultrascale XCVU440 devices providing, depending on the design to be prototyped, up to 25 million ASIC gates capacity and up to 88Mb of embedded memory per FPGA. The boards are mounted in a custom chassis with power supply, cooling and all necessary interfaces and cabling included. In addition to being equipped with a variety of on-board interfaces, the platform is complemented by a comprehensive portfolio of daughtercards and is also fully compatible with Cadence's family of SpeedBridge adapters, enabling a smooth transition from an emulation environment to a FPGA-based prototyping environment. The resulting FPGA-based prototyping portfolio is shown in figure 2. As part of the Cadence Verification Suite, FPGA-based prototyping just became easier with the Protium S1 platform. ■