Enhanced reliability and performance in motor control encoder applications

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This article focuses on key benefits for motor control applications using the 50 Mbps (25 MHz) ADM3065E RS-485 transceiver and the ADSP-CM40x mixed-signal control processor. The RS-485 transceiver is designed for reliable operation in harsh environments such as motor control encoders, with added noise immunity and (IEC) 61000-4-2 electrostatic discharge (ESD) robustness.
differences, the encoder communication protocols have similarities in regard to implementation. The interfaces of these protocols are serial bidirectional pipes that comply with either the RS-422 or RS-485 electrical specifications. While there are commonalities in the hardware layer, the software required to run each of the protocols is unique. Both the communication stack and the required application code are specific to the protocol.

This article focuses on hardware and software implementation of the master side of an EnDat 2.2 interface.

Delays fall into two categories: first, there is the transport delay of the cable, and second, there is the propagation delay of the transceivers. The speed of light and the dielectric constant of the cable determines cable delay with typical numbers of 6ns/m to 10ns/m. When the total delay exceeds half a clock period, the communication between the master and the slave breaks down. At this point, the designer has the following options: lower the data rate, bring down the propagation, introduce delay, or compensation on the master side. Option 3 compensates for both cable delay and transceiver delay and therefore is an effective way to ensure that the system can run with high clock rates on long cables. The disadvantage is that the delay compensation increases the system complexity. In systems where delay compensations are either not possible, or in systems with short cables, the value of using transceivers with a short propagation delay is evident. A low propagation delay enables a higher clock rate without having to introduce delay compensation in the system.

A master implementation consists of a serial port and a communication stack. Because the encoder protocols do not comply with standard ports, such as a UART, the peripherals found on most general-purpose microcontrollers cannot be used. Instead, the programmable logic of an FPGA enables implementation of dedicated communication ports in hardware and support of advanced features such as delay compensation. While an FPGA approach is flexible and can be tailored to the application, it also comes with disadvantages. When compared to a processor, an FPGA is costly, power hungry, and has significant time-to-market. The implementation of the EnDat interface discussed in this article is done on the ADSP-CM40x from Analog Devices, which is a processor targeting motor control drives. Besides peripherals for motor control, such as pulse width modulator (PWM) timers, analog-to-digital converters (ADCs), and sinc filters, the device has highly flexible serial ports (SPORTs). These SPORTs...
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are capable of emulating a number of protocols, including encoder protocols such as EnDat and BiSS. Because of the rich peripheral set, it is possible to perform advanced motor control, as well as interfacing to an encoder with the same device. In other words, the need for an FPGA is eliminated.

The EnDat 2.2 test setup is shown in figure 4. The EnDat slave is a standard servo motor from Kollmorgen (AKM22) with an EnDat encoder (ENC1113) mounted to the shaft. Three pairs of wires (data, clock, and power lines) connect the encoder to the transceiver board. There are two transceivers and power supply for the encoder on the EnDat PHY. One of the transceivers is used for the clock and the other transceiver is used for the data line. The EnDat master is realized with ADSP-CM40x using a mix of standard peripherals and software. Both the transmit port and receive port are implemented with flexible SPORTs.

The EnDat protocol consists of a number of different frames of varying length. However, these frames are all based on the same sequence, as seen in figure 5. First, the master issues a command to the slave, then the slave processes the command and performs the necessary calculations. Finally, the slave sends the result back to the master. The transmit clock (Tx CLK) is generated by the processor ADSP-CM40x. Because of delays in the system, the data from the encoder will be out of phase with the transmit clock before they get back to the processor. To compensate for transport delay, tDELAY, the processor also issues a receive clock (Rx CLK), which is delayed by tDELAY compared to the transmit clock. Bringing the receive clock in phase with the data received from the slave is an effective way to compensate for the transport delay.

The clock signals from the processor are continuous, while the EnDat protocol specifies the clock must only be applied to the encoder during communication. At all other times the clock line must be held high. To handle this,
the processor generates a clock enable signal, CLK EN, which is fed to the ADM3065E data enable pin. After exactly two clock periods (2T) the master starts clocking out the command on Tx DATA. The command is 6 bits long and is followed by two 0 bit. To control the data direction through the transceiver, the processor sets Bit Tx/Rx EN high while transmitting.

While the slave prepares a response, the system enters a wait state where the master continues to apply clocks, but the data line is inactive. When the slave is ready to respond, the data line receive data is pulled high and the response is sent immediately after. After receiving the n bits response, the master stops the clock by setting CLK EN signal low. At the same time, the ENC CLK signal goes high. The data flow is half duplex and the traffic on the combined data line is shown as ENC data. Figure 6 shows test results from the EnDat system. The clock frequency used in the test is 8 MHz and the delay compensation is achieved by phase shifting the receive clock. The bottom signal is the command from the EnDat master. The command shown here is send position, which is two 0s, followed by six 1s, and ended with another two 0s. In total, the command is 10 bits long. The response from the encoder is the third signal from the top. The combined data line is the second signal from the top. Finally, the top signal is the clock applied to the encoder.