Fast switching and its challenges on Power Module Packaging and System Design

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Agenda

1. Introduction fast switching
   1.1 Introduction

2. Challenges module
   2.1 Stray inductance
   2.2 Thermal performance
   2.3 Reliability

3. Challenges system
   3.1 DC link
   3.1 Electronics

4. Best practice
**Agenda**

1. **Introduction fast switching**

2. **Challenges module**
   - 2.1 Stray inductance
   - 2.2 Thermal performance
   - 2.3 Reliability

3. **Challenges system**
   - 3.1 DC link
   - 3.1 Electronics

4. **Best practice**
Fast switching

What is fast switching

10-40 kHz
- 650V/1200V
- New Si chips, new topologies, hybrid SiC
- No significant impact on module/system

>40 kHz
- 1200V/1700V
- SiC
- New challenges on module/system

Why
- Increase efficiency
- Improve modulation accuracy
- Reduction of costs
- Reduction of size

Switching with 30kV/µs and 2nH stray inductance
Challenges Power Module

**Commutation Inductance:**
Faster switching means higher di/dt resulting in higher overvoltage compared to Silicon

**Thermal performance:**
Silicon Carbide chips are smaller, give worse thermal performance compared to Silicon

**Power Cycling Capability and Reliability:**
Mechanical stress on the module interconnections is higher with SiC compared to Silicon due to its mechanical properties
Stray inductance

- Over voltage during switch-off over IGBTs/ MOSFETs
- Oscillations with chip capacitance -> EMI
- Overvoltage limits switching loss reduction by using bigger $R_G$
- Maximum usable DC link and output current is limited

Target

Reduction of stray inductance
Parasitic elements in the module

- Bond wires, DBC traces: 1...6 nH
- DC power terminals: 12...18 nH
  (busbars, DC-link: 10...30 nH)
- Module gate connectors: 20...160 nH
  (gate driver wiring: 5...20 nH)
- \( C_{\text{oss}} \): 0.2...1.5 nF/100 A
Ways for optimization for fast switching on module level

**Optimize DC+ / - terminals** regarding minimum stray inductance

Use **gate inductance** as **current booster** during Miller plateau – **smaller is not necessarily better**

**Optimize power hybrid design** regarding chips positioning, wire bonds, DBC layout...

![Diagram showing inductance comparison](image_url)
**Power Module Commutation Inductance: Fixed**

**MiniSKiiP spring contacts:**
- $L_{stray} = 20\sim$ to 30 nH
- depending on housing size, but fixed due to housing design
- 1200V/20A to 90A

**SEMITRANS screw terminals:**
- $L_{stray} = 15$ nH
- fixed due to package construction
- 1200V/350A to 500A
Power Module Commutation Inductance: Flexible

**SEMITOP E2**
Industry standard package
Pin Grid structure allows flexible placing of the Press-Fit pins

**Optimized chip layout:**
Lowest commutation inductance
$L_{stray} = 6\text{nH}$

**Super low inductive system design**
$L_{\text{stray, compl.}} = 10\text{nH}$
Vs. 45nH in std. module
Perfect layout for paralleling
Silicon Carbide is expensive:

**SiC current density is higher** than Silicon, i.e. chips are generally smaller:

- 1200V Silicon IGBT: 1A/mm²
- 1200V SiC MOSFET: 2A/mm²

**Silicon Carbide cost** is and will stay higher than Silicon

Maximum chip performance has to be maintained by **minimising the thermal resistance.**

<table>
<thead>
<tr>
<th>Ceramic substrate material</th>
<th>$\text{Al}_2\text{O}_3$</th>
<th>$\text{Si}_3\text{N}_4$</th>
<th>$\text{AlN}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal Conductivity (W/mK)</td>
<td>~25</td>
<td>~90</td>
<td>~180</td>
</tr>
<tr>
<td>Standard Thickness (mm)</td>
<td>0.38</td>
<td>0.32</td>
<td>0.63</td>
</tr>
<tr>
<td>Resulting Thermal Performance</td>
<td>100%</td>
<td>~400%</td>
<td>~400%</td>
</tr>
</tbody>
</table>
**SEMITRANS 3 Full SiC Platform**

Available in two versions, with standard Aluminium Oxide (Al$_2$O$_3$) and Aluminium Nitride (AlN).

With AlN less chips but same current at lower cost.

<table>
<thead>
<tr>
<th></th>
<th>SEMITRANS 3 Al$_2$O$_3$</th>
<th>SEMITRANS 3 AlN</th>
</tr>
</thead>
<tbody>
<tr>
<td>No. of chips per switch</td>
<td>12</td>
<td>8</td>
</tr>
<tr>
<td>Used Chip area</td>
<td>100%</td>
<td>66%</td>
</tr>
<tr>
<td>$R_{th(j-c)}$ per chip</td>
<td>0.84K/W</td>
<td>0.54K/W</td>
</tr>
<tr>
<td>Cont. drain current $I_D$</td>
<td>431A</td>
<td>416A</td>
</tr>
<tr>
<td>($T_j=175^\circ C/T_c=80^\circ C$)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Module Cost</td>
<td>100%</td>
<td>75%</td>
</tr>
</tbody>
</table>
Reliability

The publication of Technical University Chemnitz* presents the technological status as of today:

- Young modulus of SiC is bigger by a factor of 4
- SiC dies are thicker than standard Si dies
  (1200V SiC: 230µm to 330µm; 1200V IGBT4: 115µm)
- Both leads to high mechanical stress on interconnections

Expectable SiC power cycling capability is only around 33% of Silicon results in standard packages.

* Power cycling capability of Modules with SiC-Diodes, Christian Herold et.al., CIPS 2014

600V SiC-Schottky diode, compared to 1200V
IGBT, ΔTj = 81K +/- 3K and Tjmax = 145 °C +/- 5K. *
CTE mismatch to standard DBC substrates is bigger

Solution:

Use optimized DBC substrate, such as AlN for baseplate modules or Si₃N₄ for baseplate-less power modules

Better adjusted CTE and higher thermal performance.

<table>
<thead>
<tr>
<th>Material Substrate/Chip</th>
<th>Al₂O₃</th>
<th>Si</th>
<th>AlN</th>
<th>SiC</th>
<th>Si₃N₄</th>
</tr>
</thead>
<tbody>
<tr>
<td>Coefficient of Thermal Expansion (ppm/K)</td>
<td>8.3</td>
<td>4.1</td>
<td>5.7</td>
<td>3</td>
<td>2.5</td>
</tr>
</tbody>
</table>

SEMITRANS 3 Full SiC has full power cycling performance with AlN substrate.

SEMITOP E2 SiC under testing
Reliability

Young modulus of SiC is bigger by up to a factor of 4 / Most SiC chips are thicker than standard Silicon chips

Solution: Sintered Die Attach

- Fine silver paste is sintered under **40MPa pressure at ~250°C**
- **Low homologous temperature:** ratio of operation temperature to melting temperature in K
- Excellent long term reliability, *eliminating the solder layer as the weakest link.*
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Inductance – to be considered in system context

Evaluation Factor:
\[ L_{\text{STRAY}} \times I_N \]

**SKM400GB12T4**  
400A \times 15 \text{nH} = 6

**SKiiP38GB07E3V1**  
300A \times 15 \text{nH} = 4

**SKiiP25ACM12V17**  
90A \times 20\text{nH} = 1.8

**SKAI LV**  
350A \times 3\text{nH} = 1
Low inductive DC link

**How to**

- Integrate snubber capacitors -> DC Link-snubber oscillations
- Short distance between DC +/-
- Maximum overlap of DC+/-
- Paralleling of pins (power pins/bars of module and capacitors)

\[ L_{DCBusbar} \approx \mu \times a \times \frac{d}{b} \]
\[ L_{cap} \approx L_{single}/\text{capacitors} \]
Challenges

- \( \frac{dv}{dt} > 100 \text{kV}/\mu\text{s} \) with \( f_{SW} > 300 \) kHz
- \( Q_G \sim \text{Si} \), \( f_{SW} \) much higher
  - \( \rightarrow I_{\text{out ave}} \) up to 1A
- Lower \( t_{\text{dead}} \) required due to higher \( f_{SW} \)
- Fast \( V_{ce} \) detection required due to lower short-circuit withstand times
- Lower gate threshold voltage requires safe off-hold
- \( f_{SW} \) higher \( \rightarrow \) More impact of gate path inductance on oscillations
SiC MOSFETs **body diode** has a **pn-junction** and therefore **reverse recovery losses**.

**SiC Schottky** free-wheeling diode has **no reverse recovery** and reduces the overall switching losses by 30 to 40% compared to MOSFET-only topologies.

Optimising the interlock time to 120 to 300ns achieves similar results.
SKYPER used for driving SiC

<100kHz: SKYPER 42LJ
- \( \frac{dv}{dt} \) up to 100kv/\( \mu \)s
- Stabilized gate voltages
- Configurable input filter concept
- Configurable interlock
- Fast error detection <1\( \mu \)s
- Direct \( \mu \)C connection with differential 5V interface
- Over temperature, under voltage, short circuit

>100kHz dedicated research driver with 20ns input filter and special fast output stage will be used; proved at 300kHz
Best practice examples

MiniSKiiP SiC stack – 25kW
  – SKiiP 26ACM12V17
  – 600V/40A total losses 0.9mJ

SEMIKUBE SL Hybrid SiC – 100kW
  – SKM200GB12F4SiC
  – Twice the switching frequency @ same output current

19“ DC fast charger rack – 50kW
  – Low inductive SEMITOP E2
  – AFE and DC/DC converter
  – Efficiency >97%
Thank you for your attention!