Rdyn in hard and soft-switching applications

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References:


**GaN High Electron Mobility Transistor**

**GaN Material**
Binary Crystal

Spontaneous Polarization due to electro-negativity difference between N-atoms and Ga-atoms

N=3.4, Ga=1.8

**AlGaN layer**

Higher Spontaneous Polarization

N=3.4, Ga=1.8, Al=1.6

Piezoelectric polarization due to strained layer

2DEG: Ns HEMT ns~ $10^{13}$ cm$^{-2}$

(Typical MOSFET ns~ $10^{12}$ cm$^{-2}$)

**Low Ron**

high 2DEG $n_s$ ~ $1 \times 10^{13}$ cm$^{-2}$

high 2DEG mobility ~ 2000 cm$^2$/Vs

**High Breakdown**

wide bandgap (3.4 eV)

**Low Capacitance**

no junctions (undoped)

**No Qrr**
JEDEC Standard for Power Discrete Qualification:

- Semiconductor Power discretes are currently qualified based on the JEDEC Standard (JESD47/JEP122) developed for Silicon (Different activation energies for GaN so different testing conditions/models needed)
- The Statistical methods used to calculate failure rates are based on field returns and well identified failure modes (Limited knowledge built on GaN)
- The JEDEC standard does NOT provide any dynamic testing conditions, (The stability of dynamic electrical performance are crucial for GaN)

How to release GaN Power Devices to the market

<table>
<thead>
<tr>
<th>Type</th>
<th>Test</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td><strong>Device</strong></td>
</tr>
<tr>
<td></td>
<td>HTRB*</td>
<td>High Temperature Reverse Bias</td>
</tr>
<tr>
<td></td>
<td>HTGB*</td>
<td>High Temperature Gate Bias</td>
</tr>
<tr>
<td></td>
<td>HTOL</td>
<td>High Temperature Operating Life</td>
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<tr>
<td></td>
<td>LU</td>
<td>Latch-up</td>
</tr>
<tr>
<td></td>
<td>ED</td>
<td>Electrical Characterization.</td>
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<tr>
<td></td>
<td>IOL*</td>
<td>Intermittent operating life</td>
</tr>
<tr>
<td></td>
<td>AC</td>
<td>Unbiased autoclave 121C/100%RH</td>
</tr>
<tr>
<td></td>
<td>HAST</td>
<td>Biased HAST, 130C/85%RH</td>
</tr>
<tr>
<td></td>
<td>HTS</td>
<td>High Temperature Storage</td>
</tr>
<tr>
<td></td>
<td>TC</td>
<td>Temperature Cycle, -65/150C</td>
</tr>
<tr>
<td></td>
<td>ESD</td>
<td></td>
</tr>
<tr>
<td></td>
<td>HBM</td>
<td>ESD - Human Body Model</td>
</tr>
<tr>
<td></td>
<td>CDM</td>
<td>ESD - Charged Device Model</td>
</tr>
</tbody>
</table>

Graphs showing lifetime vs. temperature with Ea=2.1 eV [Whitman 2014]
New JEDEC Standard required for GaN

JC-70.1: GaN Power Electronic Conversion Semiconductor Standards:

- **Accelerate the Maturity of the Industry by Creating Credible Standards for GaN learning from the Past, Ramp Faster and Lower Risk to Customer**

- **Focus on Application & Usage in End Equipment and NOT on Harmonizing Devices, Process Equipment**

(Source: S.W. Butler, ‘Standardization for Wide Band Gap Devices: GaNSpec DWG’, APEC 2017)
GaN Quality Assurance vision

Structured Progressive Quality Assurance

QUALITY ASSURANCE

QUALIFICATION

INTRINSIC

GaN specific

Si (JESD47/AEC-Q101)

EXTRINSIC

GaN specific

Si (JESD47/AEC-Q101)

Design SOA

Screening

Failure Modes
- Field Returns (FIT)
- Test-to-Failure (FIT)

Application Mission Profile
- Electrical
- Temperature
- Ruggedness

Reliability Physics Characterization & Modeling
- Traps
- Acceleration
- Failure Modes
GaN HEMT Safe Operating Area

- Limitations of the Time Dependent Safe Operating Area:

  - Electromigration (Jmax) at Tambient/Tjunction
  - Gate Reliability
    - Vgs max.
    - Vgs min.
  - Impact of the switching modes
  - Hard Switching
  - Soft Switching
  - Dynamic Ron
  - Max. Pulsed Drain Current
  - Hot Carrier Injection
  - Max. Allowed Voltage
  - Load Profile
  - Cumulated time
  - Short-circuit capability
  - HT Reverse Bias
  - UIS Capability
  - Reliability of the GaN Epi
1 Reliability of the GaN Epi

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Reliability of the GaN Epi Buffer

- GaN Buffer behaves as a leaky dielectric
  - One $V_{\text{TLF}}$: one dominant trap [Lampert, PhysRev1956]. In our case $C_N$
  - Above $V_{\text{TLF}}$: steep voltage acceleration ($V^n$) due to Poole Frenkel

- Stressed at $T=200^\circ\text{C}$
- Acceleration Model built & verified
Impact of the Switching Modes

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What are typical Applications for GaN?

- Qualifying a product requires understanding its applications.
- Typical application of GaN includes the following:
  - Boost/Buck converter
  - Inverter
  - Bridgeless PFC
  - etc
- Most of the time GaN is hard-switched → Standard test vehicle requiring hard-switching testing is required.
DGD/Drain-Gate-Delay is referred to the overlap of the drain and gate voltage during OFF to ON switching cycle.

- Positive DGD → Towards Soft switching condition
- Negative DGD → Towards Hard switching condition
  - Higher the absolute magnitude, harsher is the condition.

**Hard-Switching Test Vehicle**

- $V_{DSQ} = 600V$
- $t_{off} \approx 2ms$
- $V_D = V_{DSQ}/2$
- $V_G = V_{th}$
- $t_{on \_DRAIN}$
- $V_{GSQ} = -20V$
- $t_{off} \approx 2ms$
- $V_G = 0V$
- $t_{on \_GATE}$
- $t_{on} = 20\mu s$
- $V_D = V_{DSQ}/2$
- $VG = V_{th}$
- $t_{on \_GATE}$
- $V_{GSQ} = (0V, 1V)$
- $V_{GSQ} = (-20V, 600V)$

**Example**

<table>
<thead>
<tr>
<th>DGD</th>
<th>Soft</th>
<th>Hard</th>
</tr>
</thead>
<tbody>
<tr>
<td>7.4 $\mu s$</td>
<td>7.4 $\mu s$</td>
<td>7.4 $\mu s$</td>
</tr>
<tr>
<td>3.3 $\mu s$</td>
<td>3.3 $\mu s$</td>
<td>3.3 $\mu s$</td>
</tr>
<tr>
<td>2.4 $\mu s$</td>
<td>2.4 $\mu s$</td>
<td>2.4 $\mu s$</td>
</tr>
<tr>
<td>1.4 $\mu s$</td>
<td>1.4 $\mu s$</td>
<td>1.4 $\mu s$</td>
</tr>
<tr>
<td>0.4 $\mu s$</td>
<td>0.4 $\mu s$</td>
<td>0.4 $\mu s$</td>
</tr>
<tr>
<td>-0.05 $\mu s$</td>
<td>-0.05 $\mu s$</td>
<td>-0.05 $\mu s$</td>
</tr>
<tr>
<td>-0.35 $\mu s$</td>
<td>-0.35 $\mu s$</td>
<td>-0.35 $\mu s$</td>
</tr>
<tr>
<td>-0.65 $\mu s$</td>
<td>-0.65 $\mu s$</td>
<td>-0.65 $\mu s$</td>
</tr>
<tr>
<td>-0.75 $\mu s$</td>
<td>-0.75 $\mu s$</td>
<td>-0.75 $\mu s$</td>
</tr>
</tbody>
</table>
Measurement Conditions

R_{LOAD} = 1kΩ

Pulsed IV (Double pulse setup):
\( V_G = -20V \)
\( V_{DD/DS} = \) from 0V to 600V, 100V/step
\( V_S = V_{chuck} = 0V \)

Hard Switching stress:
\( V_G = 0V; \)
\( V_{DD} = \) As per the stress condition
\( V_{DS} \) measured by the custom probe
\( I_{DS} = I_{RLOAD} = V_{RLOAD}/R_{LOAD} \)
\( V_S = V_{chuck} = 0V \)

Temperature: Room and High temperature

Pulsed \( I_DV_D \) → Hard Switching Stress (DGD ≈ varying) → Pulsed \( I_DV_D \)
Study of Possible Degradation

- Hard switching condition leads to a dynamic variation of the on-resistance.
- The analysis of the on-resistance variation demonstrates that:
  - Increase of the on-resistance is directly linked to decrease of DGD.
  - No degradation observed for Soft switching condition (comparable to fresh device).
  - Is the degradation off-state voltage accelerated?

\[ R_{\text{on\_variation}} = \frac{R_{\text{on\(-20,VDSQ)}}}{R_{\text{on\(0,0\)}}} \]
Is the Degradation Voltage Accelerated?

- The degradation is Voltage accelerated.
- Off-state voltage \( \geq 300V \) + decreased DGD \( \rightarrow \) significant increase of the on-resistance.

\[
R_{\text{on variation}} = \frac{R_{\text{on (-20,VDSQ)}}}{R_{\text{on (0,0)}}}
\]
Is the Degradation Temperature Accelerated?

- The dynamic variation of the on resistance changes with the ambient temperature.
  - The change of the dynamic RON for VDSQ = 200V increases with temperature, with the «Bump: shifting towards lower VDSQ.
  - At VDSQ = 600V the variation of the on-resistance slightly decreases with temperature, presumably influenced by:
    - Increase of the detrapping process with temperature, detectable at both DGD = 3.3 µs and DGD = -0.65 µs.
    - Decrease of the influence of the hot electrons, detectable mainly at DGD = -0.65 µs.
Understanding of the Degradation Mechanism?

- Device degradation under hard switching condition is caused by Hot Electrons in the channel.
  - Higher the power dissipation $\rightarrow$ Higher is the degradation.
- Recent TCAD\textsuperscript{[1]} studies reported in literature points to similar facts.
  - Gate/Field plate edges (edge effect) suffer from high E-field in off-state, leading to higher degradation in those localized areas.

\begin{tabular}{|c|c|c|}
  \hline
  & $I_{DS} \sim 0 \text{ A}, \ V_{DS} = 480 \text{ V}$ & $I_{DS} \sim 5 \text{ A}, \ V_{DS} = 480 \text{ V}$ \\
  \hline
  \textbf{E-field} & \includegraphics[width=0.4\textwidth]{E-field_0A.png} & \includegraphics[width=0.4\textwidth]{E-field_5A.png} \\
  \textbf{Electron density} & \includegraphics[width=0.4\textwidth]{Electron_density_0A.png} & \includegraphics[width=0.4\textwidth]{Electron_density_5A.png} \\
  \textbf{Hot-carrier Generation} & \includegraphics[width=0.4\textwidth]{Hot-carrier_0A.png} & \includegraphics[width=0.4\textwidth]{Hot-carrier_5A.png} \\
  \hline
\end{tabular}

Emission Microscopy Results [1]

- Spatially resolved EL spectra confirms the hot electron related degradation during hard switching.
  - Decreasing DGD $\rightarrow$ Higher EL signal $\rightarrow$ Higher degradation.
  - No emission observed for soft switching condition.

- EL/Degradation signal is observed at the gate edge of the drain side.
  - Results in line with TCAD understanding.

<table>
<thead>
<tr>
<th>DGD</th>
<th>Drain Gate DGD</th>
<th>Drain Gate DGD</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.4 µs</td>
<td>-0.4 µs</td>
<td>-0.75 µs</td>
</tr>
<tr>
<td>-0.4 µs</td>
<td>-0.85 µs</td>
<td>-0.9 µs</td>
</tr>
<tr>
<td>-0.75 µs</td>
<td>-0.95 µs</td>
<td>-1 µs</td>
</tr>
</tbody>
</table>

Soft Switching (DGD=3.3 us)

Hard Switching
Good correlation is noticed between the increase of the EL signal and of the dynamic on resistance.

- Dynamic RDS$_{on}$ increase can be attributed to hot carrier type of degradation occurring in the access region (gate-drain).
Is the Degradation Recoverable?

- Comparison of EL spectra before and after hard switching stress measurement demonstrates no permanent degradation.

\[
DGD = -0.81\mu\text{s} \quad V_{DSQ} = 600\text{V}
\]

EL signal under hard switching stress

\[
DGD = 3.3\mu\text{s} - \text{BEFORE}
\]

\[
DGD = 3.3\mu\text{s} - \text{AFTER}
\]
Electro-luminescence as a means to define SOA

- Two identical device layouts, different buffers (optimization for dyn Ron, lateral leakage current etc...)

![Graphs showing electro-luminescence](image-url)
A successful methodology is established for reliability assessment of GaN.

- Initial demonstration on single finger devices shows good correlation with understanding (& TCAD).
- Measurement setup can be easily adapted (high flexibility) for powerbar measurements.
- Tests are done at wafer level → Fast feedback

High power dissipation during a hard-switching event is one of the major degrading factors for GaN power devices.

- Hot electrons accelerated under high off-state bias leads to trapping in access regions → Dynamic $R_{DS_{on}}$ increase.
- Higher the power dissipation during hard-switch event = Higher is the $R_{DS_{on}}$ increase.
- This degradation is NOT permanent
- Degradation can be reduced by proper device architecture (such as Field Plate design, etc)
Conclusions

• ON Semiconductors’ vision on Quality Assurance for GaN based power systems is presented:
  – Si JEDEC qualification to be extended with GaN specific tests, e.g. on Rdyn
  – Design SOAs are developed, supporting application mission profiles
  – Extensive screening tests are mandatory in the early years

• As an example, Rdson dispersion (Rdyn) is studied:
  – Impact demonstrated of hard switching vs soft switching applications.
  – SOA Design rules, enabling product design for high reliability applications

• Collective learning to result in a new Jedec standard specifically for GaN (JC-70).