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Xilinx Zynq-7000 Extensible Processing Platform with Dual ARM Cortex-A9 processors – a field report

Speaker: Stefan Purr, Heitec

Abstract

This presentation gives a short summary of the experiences which Heitec made with the transition from former Xilinx PPC/MicroBlaze Embedded Systems with PLB-Bus to the new Xilinx Zynq-7000 Extensible Processing Platform (EPP). The Xilinx Zynq-7000 EPP is based on Dual ARM Cortex-A9 processors and AXI-Interconnect.

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Agenda

- **The Company HEITEC**
- **Former HEITEC Projects with Xilinx PPC/MicroBlaze Embedded System and PLB-Bus**
- **Zynq-7000 Extensible Processing Platform (EPP) Architecture Overview**
  - Zynq-7000 EPP Block Diagram / Highlights
  - Processor System (PS)
  - Programmable Logic (PL)
- **AXI-Interconnect Overview**
  - AXI4
  - AXI4-LITE
  - AXI4-Streaming
- **Zynq-7000 EPP Design Flow / Experiences gained from HEITEC first Zynq-7000 EPP Test Design**
- **HEITEC Customer Concept Study – External Processor + FPGA <-> Zynq-7000 EPP One Chip Solution**
- **Summary**

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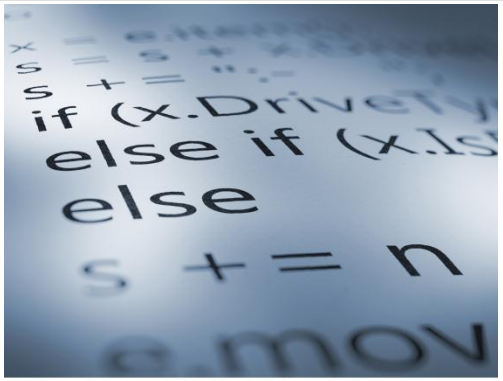

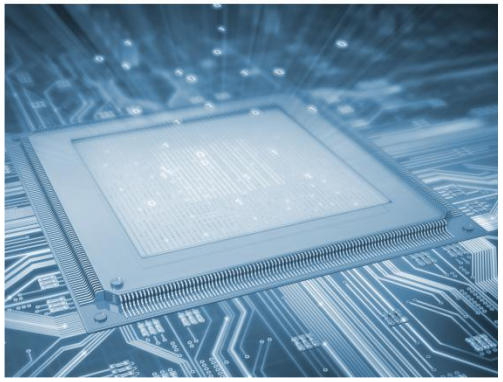

The Company HEITEC

systems provider for integrated industrial solutions

more than 25 years of engineering experience

core competence in electronics, software and mechanics

over 850 highly-qualified employees at 24 locations, 17 of it in Germany

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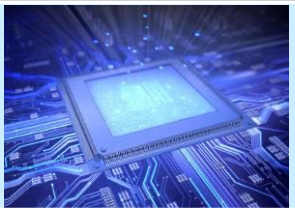
Electronic System Design – Industries & Expertise

Computing	Industrial	Healthcare	Semiconductor
- Enterprise Server - Industrial PCs - High Perf. Computing - Embedded Computing	- Automation Systems - Motion Control - Measurement	- CT/MR Data Acquisition - Wireless Communication - Hearing Aid	- Chip Design - Chip Verifikation - EMC Consulting
			
Telecom	**Automotive**	**Aerospace**	**Energy**
- Optical Networks - Mobile Base Stations - ATCA Systems - Powerline	- Car Infotainment - ECUs - EMC Consulting	- Doors & Slide Control - HPC Platform - Data Recorder - Requirement Mgmt.	- Wind Park Control - Power Monitoring - Nuclear Power Plants
			

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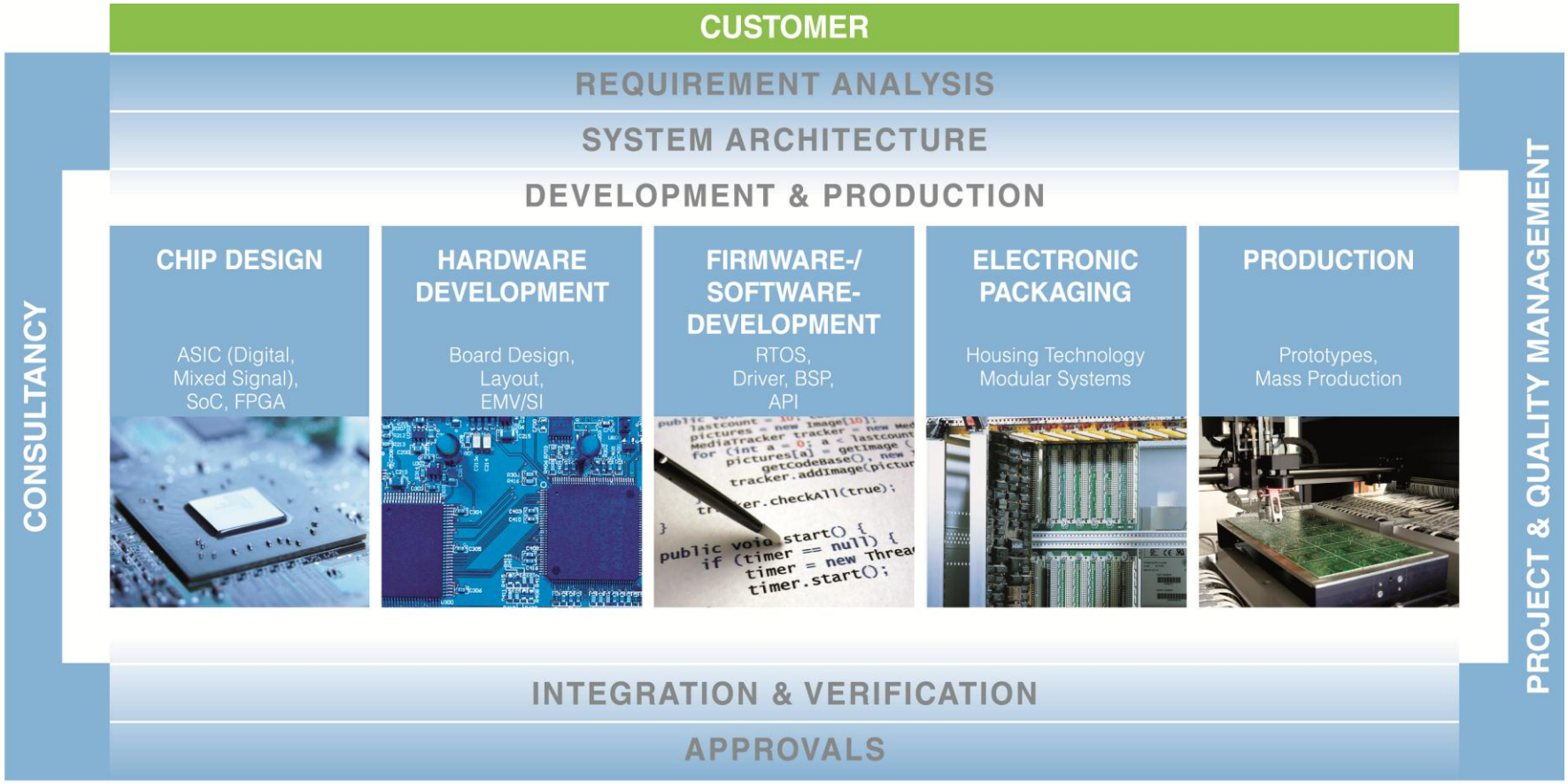
Electronic System Design – Competences



Product Lifecycle Management: From the initial concept to product discontinuation. HEITEC AG is at your side during all project phases.

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Former HEITEC Projects with Xilinx PPC/MicroBlaze Embedded System and PLB-Bus

- Distributed Imaging System with MicroBlaze Embedded System (Virtex-6)
- X-ray Detector Module with MicroBlaze Embedded System (Virtex-6)
- Aircraft Electronic Data Recorder with Power PC 440 (Virtex-5)

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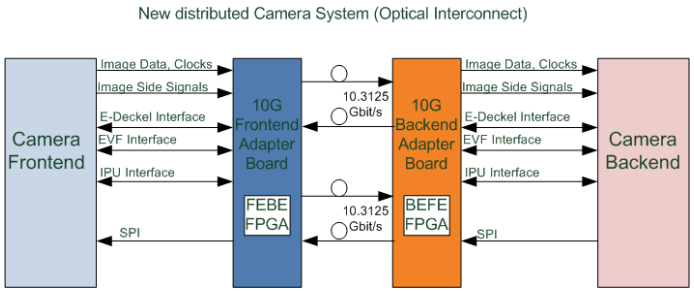
Distributed Imaging System 2x10G



- **Topic – Image Data Processing**
  Distributed Imaging System for Image & Control Data Transmission via 2x10 Gbit/s optical links for the cine camera system ARRI AlexaM – Turn-Key Project
- **Functions**
  - MicroBlaze Embedded Microcontroller
  - 333.33 MHz DDR3 SDRAM Interface
  - 175 MHz 64 bit DDR Image Data ADC Interface w. ISERDES/OSERDES
  - 2 x XAUI Interface, 8 x 3.125 Gbit/s Serial I/O
  - 1 Gbit SGMII Ethernet Interface
  - SPI, I2C, CAN, UART Interfaces
- **Device**
  - Virtex-6 CX130T-2 / FF784
- **Effort**
  - Team Size: 3-5 engineers
  - Time Frame: app. 6 months

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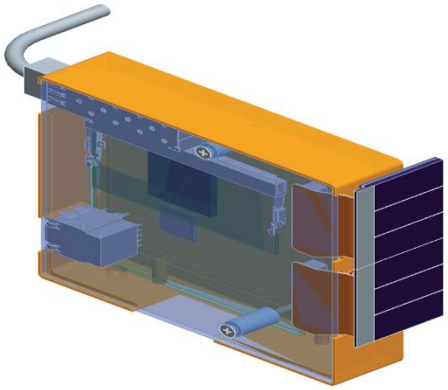
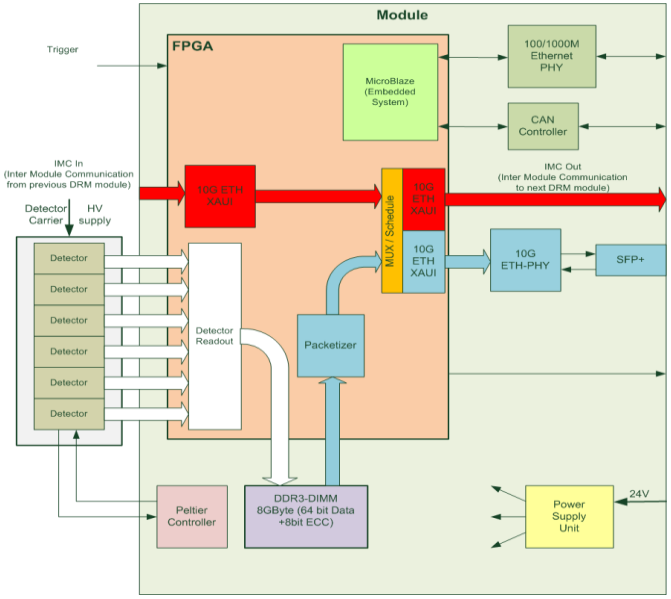
X-ray Detector Data Readout Module





- **Topic – Medical / CT**
  Data Readout Module for X-ray Detector Application for Breast Cancer CT
- **Functions**
  - MicroBlaze Embedded Microcontroller
  - 333.33 MHz DDR3 SDRAM Interface
  - 6 x 250 MHz DDR Sensor Read Out Link
  - 3 x XAUI Interface, 12 x 3.125 Gbit/s Serial I/O
  - 333.33 MHz DDR3 8 GB SORDIMM Interface
  - 1 Gbit SGMII Ethernet Interface
  - SPI, I2C, CAN, UART Interfaces
- **Device**
  - Virtex-6 LX130T-2 / FF1156
- **Effort**
  - Team Size: 3-5 engineers
  - Time Frame: app. 7 months

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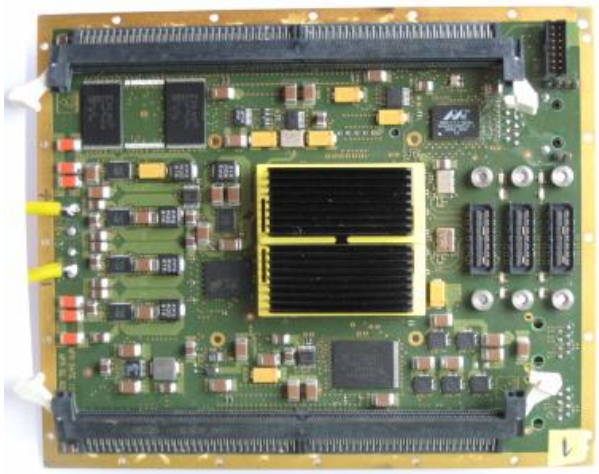
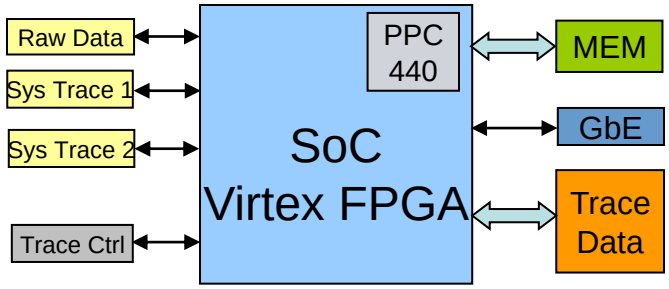
Aircraft Electronic Data Recorder





- **Functions**
  - 1,7 GB/s Aurora Interface, 10 x 2,6 Gbit/s Lanes
  - 2 x 125MB/s Serial I/O Interface
  - 1 Gbit Ethernet Interface SGMII
  - 2 x DDR2 SDRAM 64bit/150 MHz (2 x 8 GB Dual Rank RDIMM)
  - 1 x DDR2 SDRAM 16 bit/250 MHz
  - Power PC 440 / 500 MHz
  - DMA
- **Device**
  - Virtex-5 FX130 / 1738 Pins
  - 840 User-I/O
  - 125-500 MHz, 2.6 Gbit/s I/O
- **Effort**
  - Team Size: 3-5 engineers
  - Time Frame: app. 8 months

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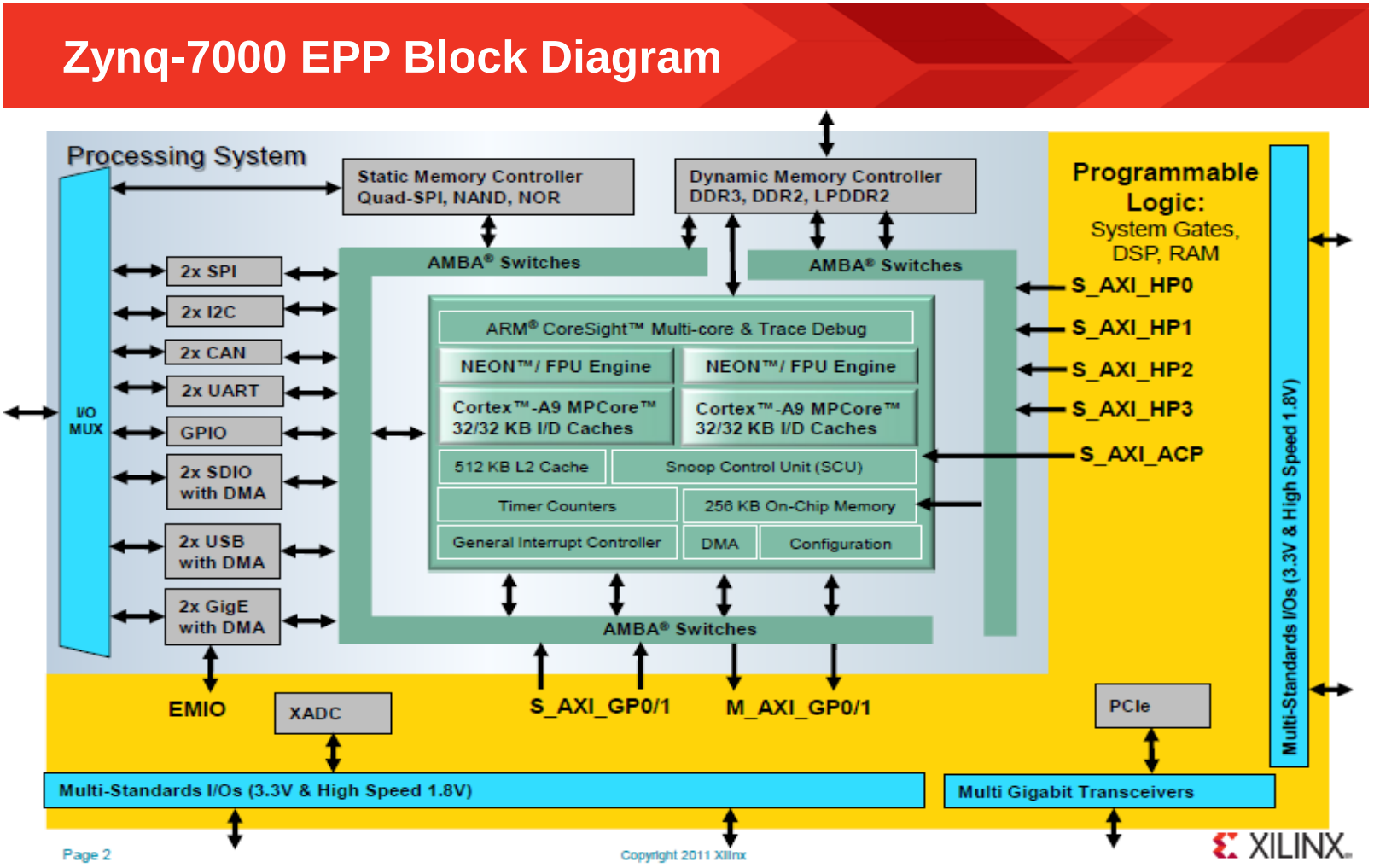
Zynq-7000 Extensible Processing Platform Architecture Overview

- Zynq-7000 EPP Block Diagram / Highlights
- Processor System (PS)
- Programmable Logic (PL)

Zynq-7000 EPP Block Diagram



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Zynq-7000 EPP Highlights (1)

- **One Chip ARM CPU/FPGA Solution**

- **Complete ARM-based Processing System**
  - Dual ARM Cortex-A9 MPCore (Frequency up to 800 MHz)
  - 2.5 DMIPS/MHz per CPU core
  - L1 Cache 32KB I/D, L2 Cache 512KB, on-chip Memory 256KB
  - NEON & Single / Double Precision Floating Point for each processor
  - Fully integrated and hardwired Processing System
  - Integrated memory controllers, DMA & peripherals
  - Fully autonomous to the Programmable Logic (Processor Boots first like any other CPU and can start operation even before Programmable Logic is configured)

- **Tightly Integrated Xilinx 7 Series Programmable Logic**
  - High performance AXI based Interface (9 AXI Interconnects)
  - Tight Coupling of the Processing System and Programmable Logic for high bandwidth and low latency

- **External Memory Support**
  - DDR2, DDR3 (up to DDR1333), LPDDR2, 2 x QSPI, NAND, NOR/SRAM

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Zynq-7000 EPP Highlights (2)

- **Xilinx 7 Series Programmable Logic (same as used for Artix-7/Kintex-7 FPGAs)**
  - 430K-5.2M approximate ASIC Gates / 28K-350k Logic Cells
  - Extensible Block RAM up to 2180KB
  - Up to 900 DSP blocks delivering over 1080 GMACs
  - 28 nm HPL Process (High Performance Low Power) from TSMC
  - PCI Express (Root Complex or Endpoint) Gen2 x4 or Gen2 x8
  - Dual 12 bit 1Msps A/D Converter

- **Processing System with flexible Built-in Peripherals**
  - 2 x SPI, 2 x I2C, 2 x CAN, 2 x UART, 4 x GPIO 32bit, 2 x SD/SDIO w. DMA, 2 x USB w. DMA, 2 x GigE w. DMA, NAND/NOR Flash Controller

- **Flexible Array of I/O**
  - High performance integrated Multi Gigabit Serial transceivers (Up to 16 x 12.5 Gbps)
  - Wide range of external multi-standard I/O (1.2V to 3.3V I/O)

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Zynq-7000 EPP Highlights (3)

- **Software Programming Model exactly the same as in Standard ARM-based Processing Systems**
- **Easy software migration from other ARM-based Systems**
- **Standard Operating Systems**
  - Linux, Android, WinCE, VxWorks, ENEA OSE, EL ThreadX, Mircrium uC/OSII, and many others
- **Tools and Debug Support**
  - ARM DS-5, ENEA Optima, Lauterbach TRACE32, and many others

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AXI-Interconnect Overview

- AXI4
- AXI4-LITE
- AXI4-Streaming

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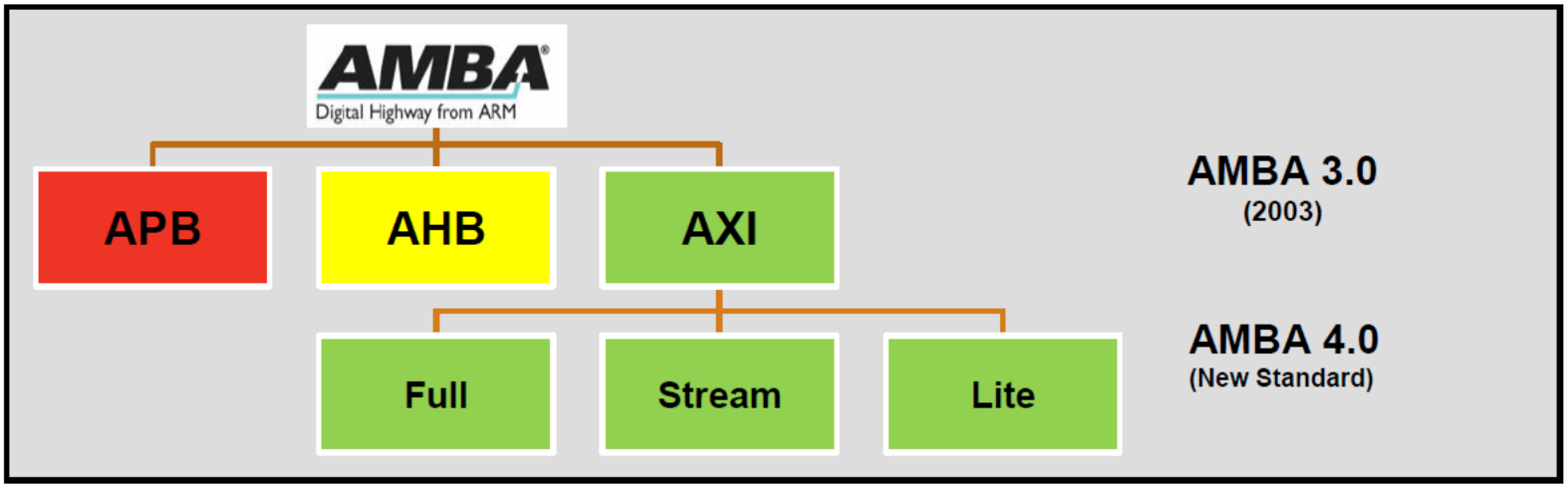
AXI Block Diagram



- **AHB (AMBA Advanced High Performance Bus)**
  - **traditional single-channel, shared bus architecture**
- **AXI (AMBA-Advanced Extensible Interface)**
  - **multi-Channel, read/write optimized point-to-point concept**
  - **high bandwidth multilayered interconnect**
  - **transaction-oriented protocol (consistent of address, data and response transfers on corresponding channel, identification by transaction ID tag)**

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AXI4 / AXI4-LITE / AXI4-Streaming

- **AXI4**
  - focus is on high performance data transfers with memory-mapped requirements
  - maximum burst length is 256 transfers (AXI3 supports 16)
  - multiple outstanding addresses, out-of-order transaction processing
- **AXI4-LITE**
  - focus is on the low-end like hardware control/status registers, etc.
  - burst length is fixed to one data transfer
  - reduced to a few basic transaction types
  - low throughput memory-mapped communications
- **AXI4-Streaming**
  - designed for high speed streaming data to destinations that are not memory-mapped internally
  - transactions do not have any address phases
  - single unidirectional channel for transmission of streaming data
  - unlimited burst (packet) length

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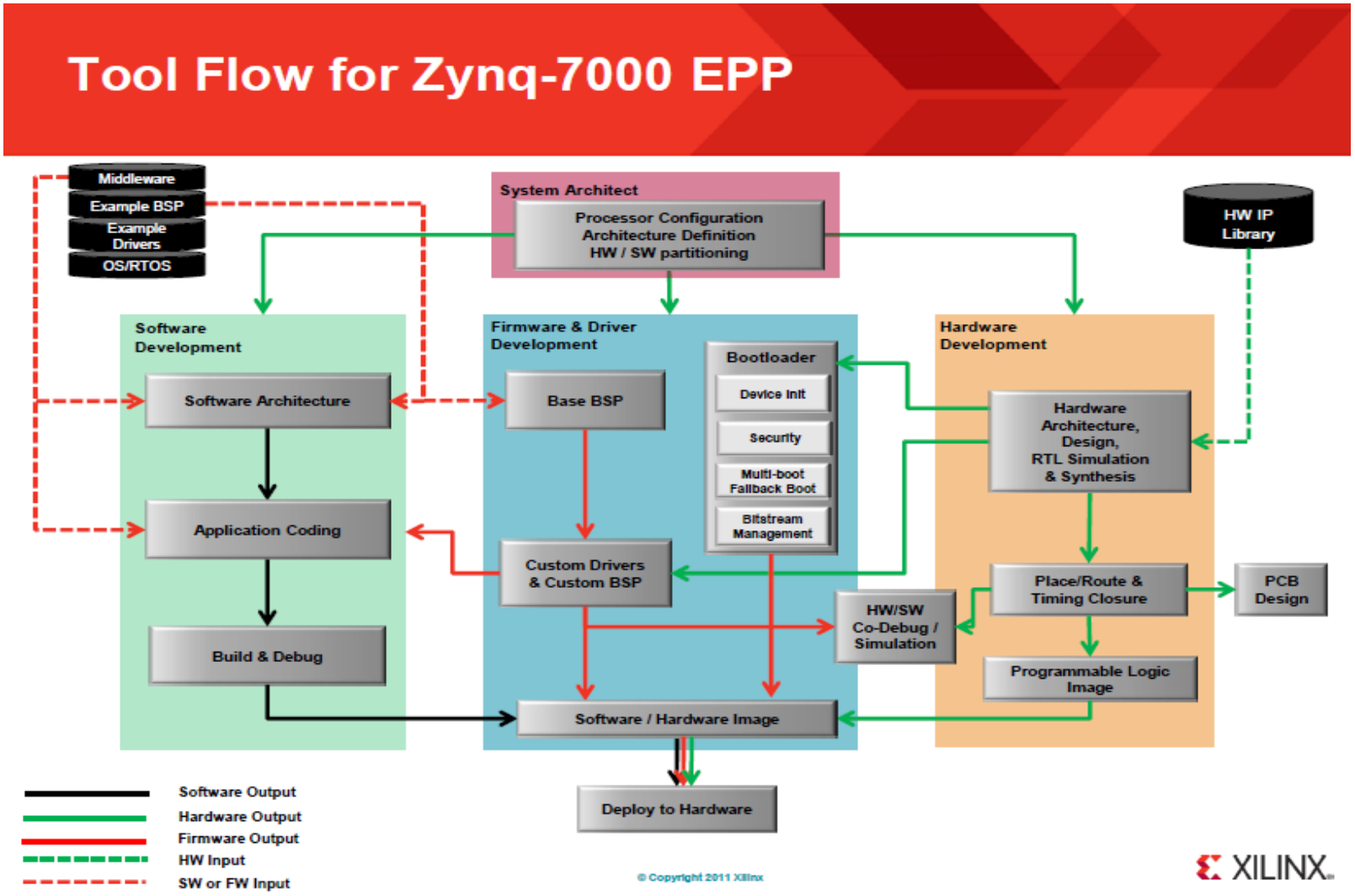

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Experiences gained from our first Zynq-7000 Test Design

- **Familiar HW design flow with Xilinx platform studio (XPS) / PlanAhead / ISE**
- **Easy to use wizards available for processor parameterization -> easier than in former MicroBlaze EDK Designs**
- **Standard Processor System is immediately alive upon Power Up**
- **Fast Software Testing possible with Xilinx Evaluation Board**
- **Fast Bring Up Time of first Zynq-7000 EPP System booting LINUX from SD Card (with Xilinx Zynq-7000 Evaluation Board)**
- **Short Development Time for own Zynq-7000 Board (Xilinx Board Files & Gerber Data from Evaluation Board available)**
- **The Flexibility and Scalability of the Zynq-7000 EPP approach provides a basis for reusing the gained experience in many future projects**

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HEITEC Customer Concept Study

- Customer Requirements
- Pros and Cons of Standard Processor + FPGA Solution
- Pros and Cons of One Chip Zynq-7000 EPP Solution

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Customer Requirements

- **Microcontroller Performance Class ARM9**
- **CPU DDR3 SDRAM Interface for 256 Mbyte SDRAM**
- **TRACE-RAM DDR3 SDRAM Interface**
- **Boot Loader with 2 Images**
- **Direct Boot from SD Card**
- **Serial NOR Flash Interface**
- **Bitstream / Software Update over Ethernet**
- **2 x Profinet / IEC61850 Interface**
- **2 x Customer specific High Speed Serial Interfaces**
- **I2C Interface for fan control**
- **A/D Converter**
- **UART/I2C/SPI peripheral Interfaces**
- **Ethernet based diagnosis Interface for Software Updates, diagnosis, trace read capability**

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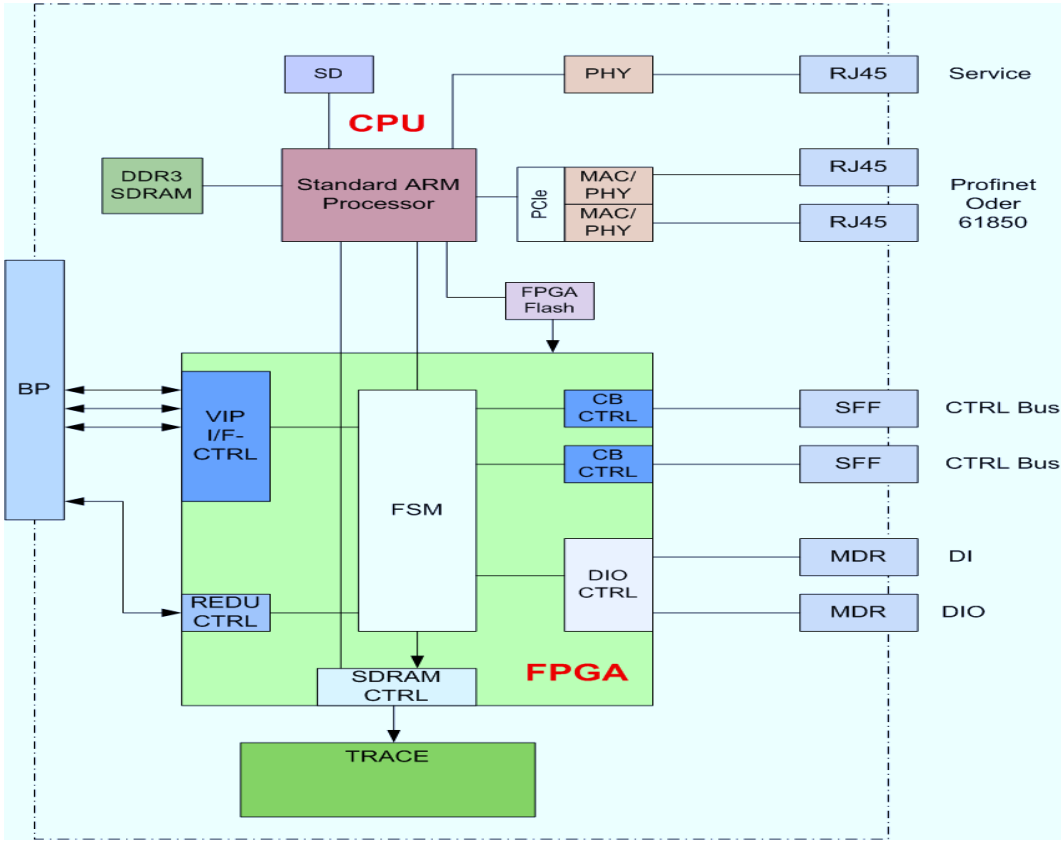
Standard Processor + FPGA Solution



pros

- established solution

cons

- external bus interface between CPU and FPGA
- less design flexibility
- less performance due to limited I/O Bandwidth / Latency
- higher pcb risk / cost
- shorter long term availability
- higher total power
- higher unit cost

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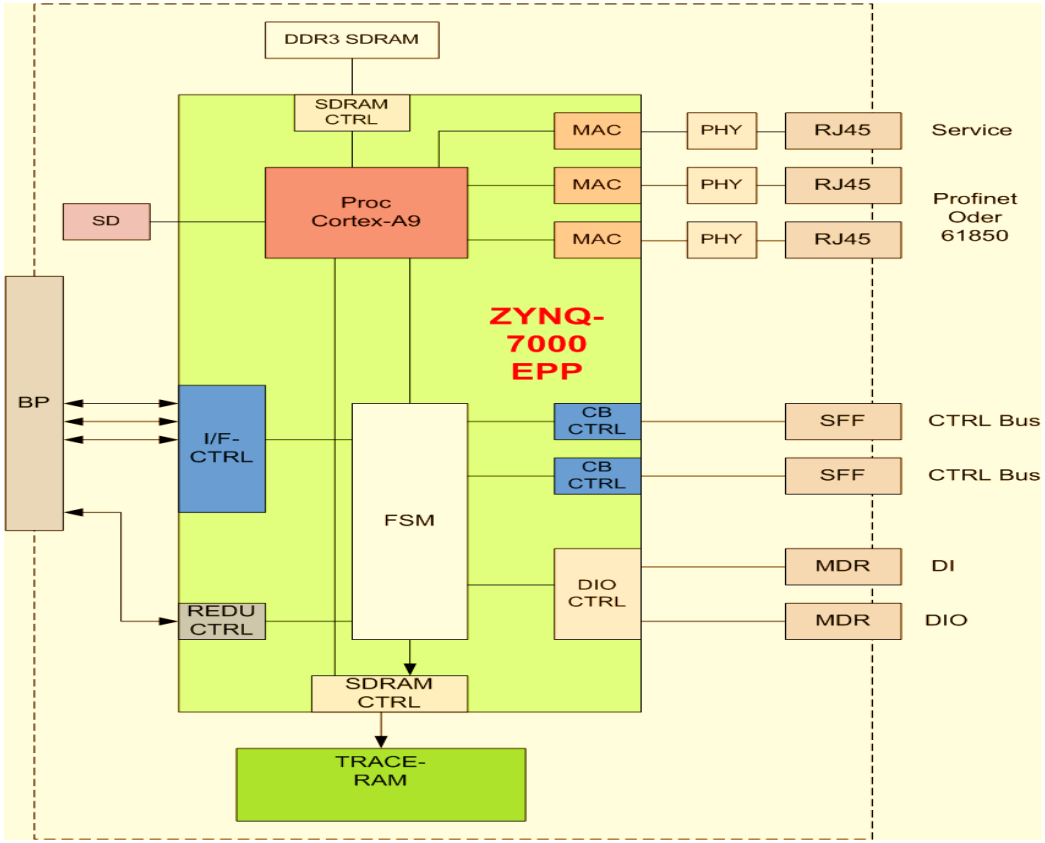
One Chip Zynq-7000 EPP Solution



pros

- design flexibility
- reduced pcb risk
- pcb component reduction
- simple & straight solution
- high performance internal AXI bus interface between CPU and Programmable Logic (tight coupling)
- debug possibilities
- long term availability
- significant total power reduction
- unit cost reduction

cons

- new component & concept

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Summary

- **Complete Standard ARM-based fixed Processing System with tightly integrated Xilinx 7 Series 28 nm Programmable Logic**
- **Single Chip Solution optimized for system-cost, power and size**
- **High-performance, low-latency signal processing solution with great capabilities according to extension, scalability and flexibility**
- **Easy to use standard software programming environment and model**
- **ZYNQ-7000 EPP offers the flexibility and scalability of an FPGA paired with the performance, power and ease of use of Standard Processor or ASIC Solutions**

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